

PROJECT NAME : CAL51/CLA61/CAL71
PCB NO :

Dell / Compal Confidential

Schematic Document

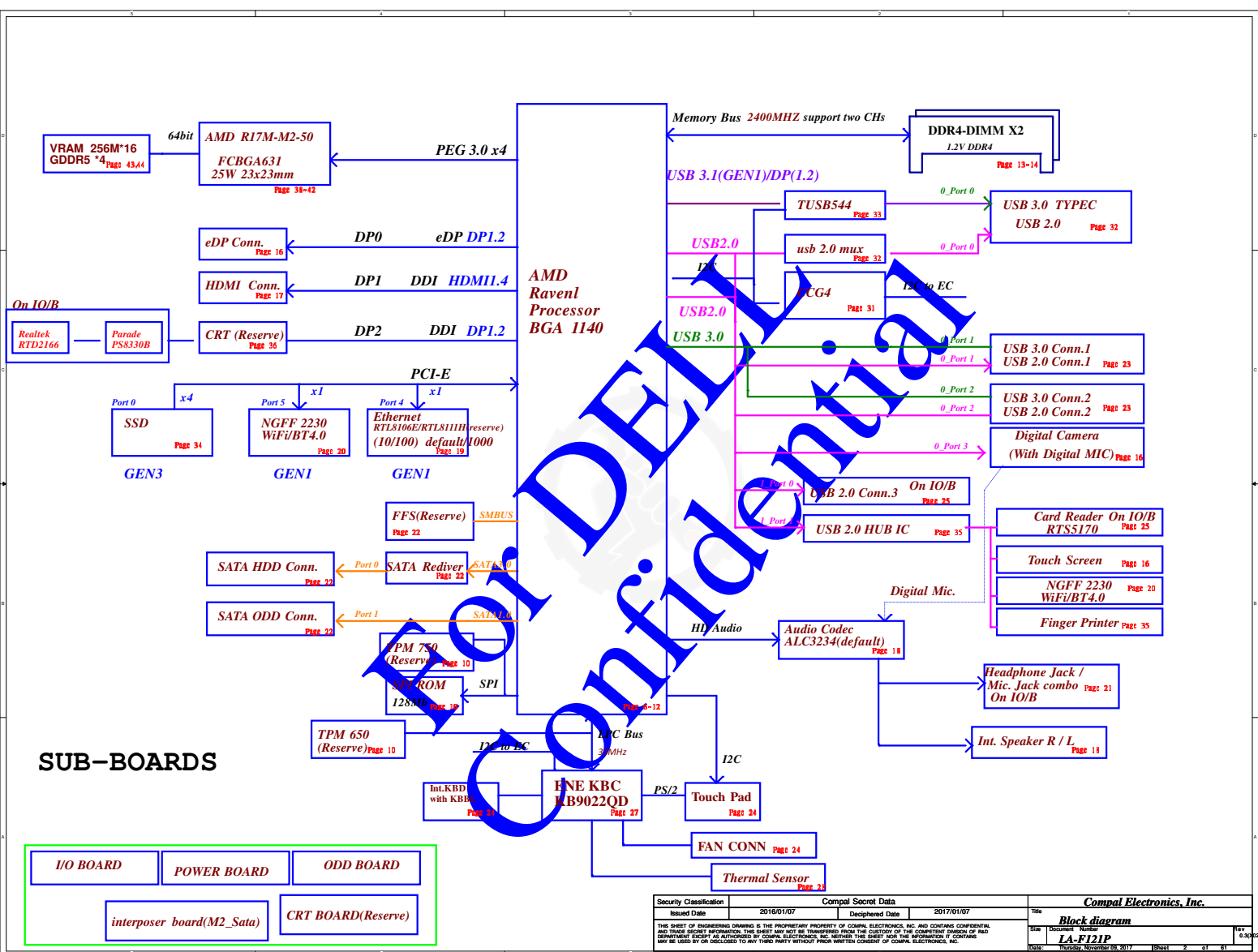
AMD Raven

AMD R17M-M2-50 (23 X 23mm)+GDDR5 x4

2017-11-09 Rev: 1.00 (A00)

@ : Un-pop Component
R5_PC@/R7_PC@/R3_PC/R5_PR@/R7_PR@/R5_PR_R3@/R7_PR_R3@:APU PN
45@: HDMI LOGO
PCB@/: MB part number
4G_S@/4G_M@/4G_H@/2G_H@/2G_M@/2G_S:
VRAM Strap Pin:
Vram 2G:S2G_R3@ / H2G_R3@ /M2G_R3@
Vram 4G:S4G_R3@ / H4G_R3@ /M4G_R3@
DIS@ GPU only
M50_R3@:GPU R3 PN
UMA@/:UMA only
TI@/PARADE@/NRDSA@ : SATA
3234@ :Audio
EMI@/ESD@/RF@ : EMI, ESD ,RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD,RF unpop
KBBL@:for KB backlight use
PTP@/NPTP@/TF_WAKE@:Touch pad
TYPEC@/NOTYPEC@:TYPEC
Typec@EMI@/Typec@ESD@: EMI/ESD typec component
CRT@:D-sub TPM@:TPM FFS@:free fall sensor
HDT@ /Debug use
MODS@:moderd standby

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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				LA-F121P
				Rev. 0.30
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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC_AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table

Board ID	
0	Raven EVT UMA
1	Raven EVT DIS
2	Raven DVT1 UMA
3	Raven DVT1 DIS
4	Raven DVT2 UMA
5	Raven DVT2 DIS
6	Raven Pilot UMA
7	Raven Pilot DIS
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

SMBUS Control Table



	SOURCE	BATT	Charger	DIMM	Thermal Sensor	FFS	CRT
EC_SMB_CK1 EC_SMB_DA1	KB9022Q	V	V				
EC_SMB_CK2 EC_SMB_DA2	KB9022Q				V		
EC_I2C_TPCLK EC_I2C_TPDAT	KB9022Q						
APU_SCLK0 APU_SDATA0	APU			V		V	V
APU_SCLK1 APU_SDATA1	APU						
APU_SIC APU_SID	APU				V		

PCI EXPRESS(GFX)

Lane 1	PEG (AMD)M2-50
Lane 2	PEG (AMD)M2-50
Lane 3	PEG (AMD)M2-50
Lane 4	PEG (AMD)M2-50
Lane 5	RV2 NA
Lane 6	RV2 NA
Lane 7	RV2 NA
Lane 8	RV2 NA

RV2 NA	USB3.0	
	0_Port0	TYPE C
	0_Port1	USB3 connector 1
	0_Port2	USB3 connector 2
	0_Port3	progaming DP signal
	1_Port0	
	1_Port1	
	USB2.0	
	0_Port0	TYPE C
	0_Port1	USB connector 1
ULT	0_Port2	USB connector 2
	0_Port3	Camera
	1_Port0	USB connector 1(D/B)
	1_Port1	USB HUB
	PCI EXPRESS(GPP)	
	Lane 1	NVME SSD
	Lane 2	NVME SSD
	Lane 3	NVME SSD
	Lane 4	NVME SSD
	Lane 5	10/100 LAN(GIGA RESERVE)
RV2 NA	Lane 6	NGFF Card (WLAN)
	Lane 7	use sata interface
	Lane 8	use sata interface
	SATA	
	SATA0	HDD
	SATA1	ODD

Symbol Note :

 : means Digital Ground
 : means Analog Ground

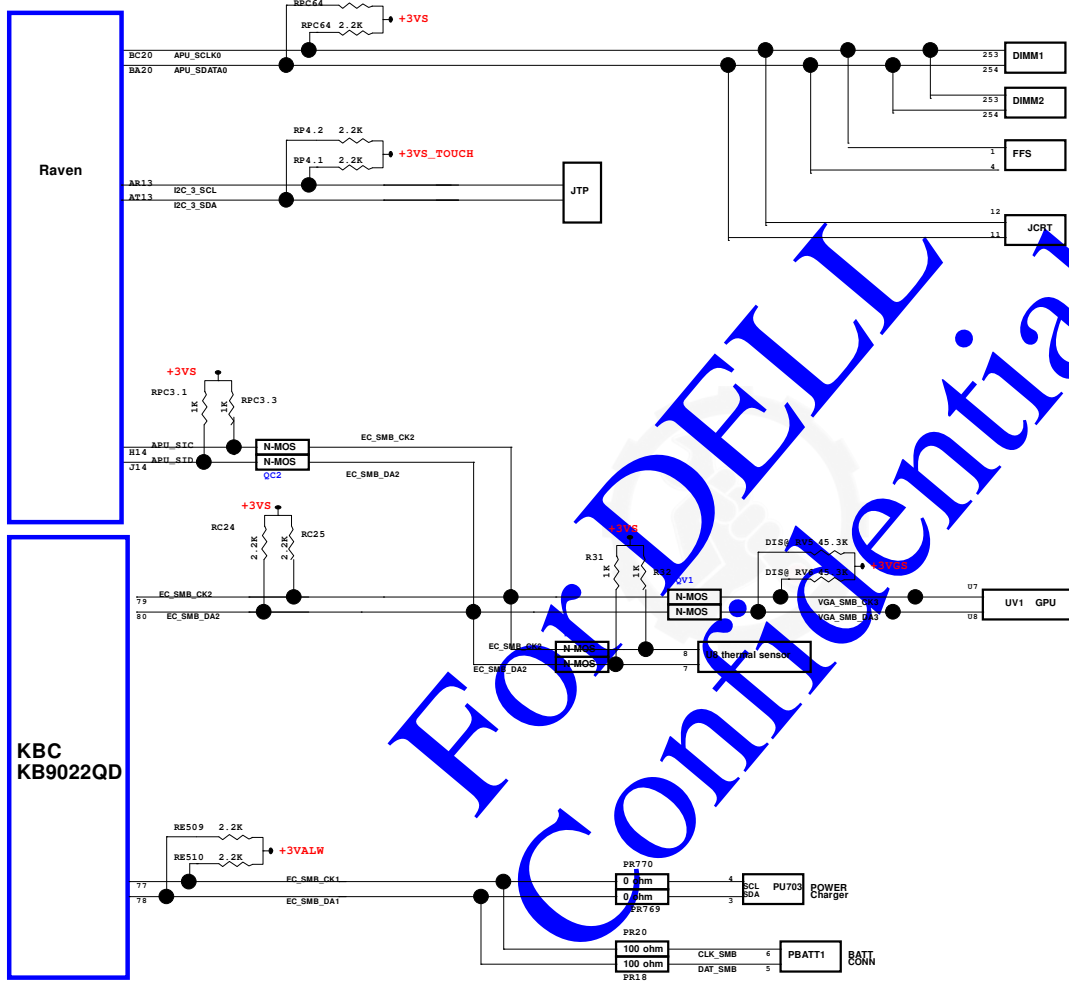
Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+SDC_IN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or DC for power circuit	N/A	N/A	N/A
+APU_VDDCORE	Core voltage for APU	ON	OFF	OFF
+APU_VDDSOC	VDDSOC voltage for APU	ON	OFF	OFF
+3VALW_APU	3V, always for APU	ON	ON	ON
+0.8VALW_APU	0.8V, always for APU	ON	ON	ON
+1.8V_ALW_APU	1.8V, always for APU	ON	ON	ON
+0.8VS	0.8V, sustain for APU	ON	OFF	OFF
+VGA_CORE	VGA core power rail for GPU	ON	OFF	OFF
+1.35V_MEM_GFX	+1.35VS power rail for GPU and VRAM	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	0.95V power rail for GPU	ON	OFF	OFF
+3.3V_VDD_PIC	3.3V power rail for PD chip	ON	OFF	ON*
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VS	System +3VS power rail	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1.2V_DDR	DDR4/L-RS +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4/L-RS +2.5V power rail	ON	ON	OFF
+1.8VS	System +1.8VS power rail	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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				Size Document Number
				LA-F121P
				Date: Thursday, November 09, 2017 Sheet 4 of 61

SMBus Block Diagram

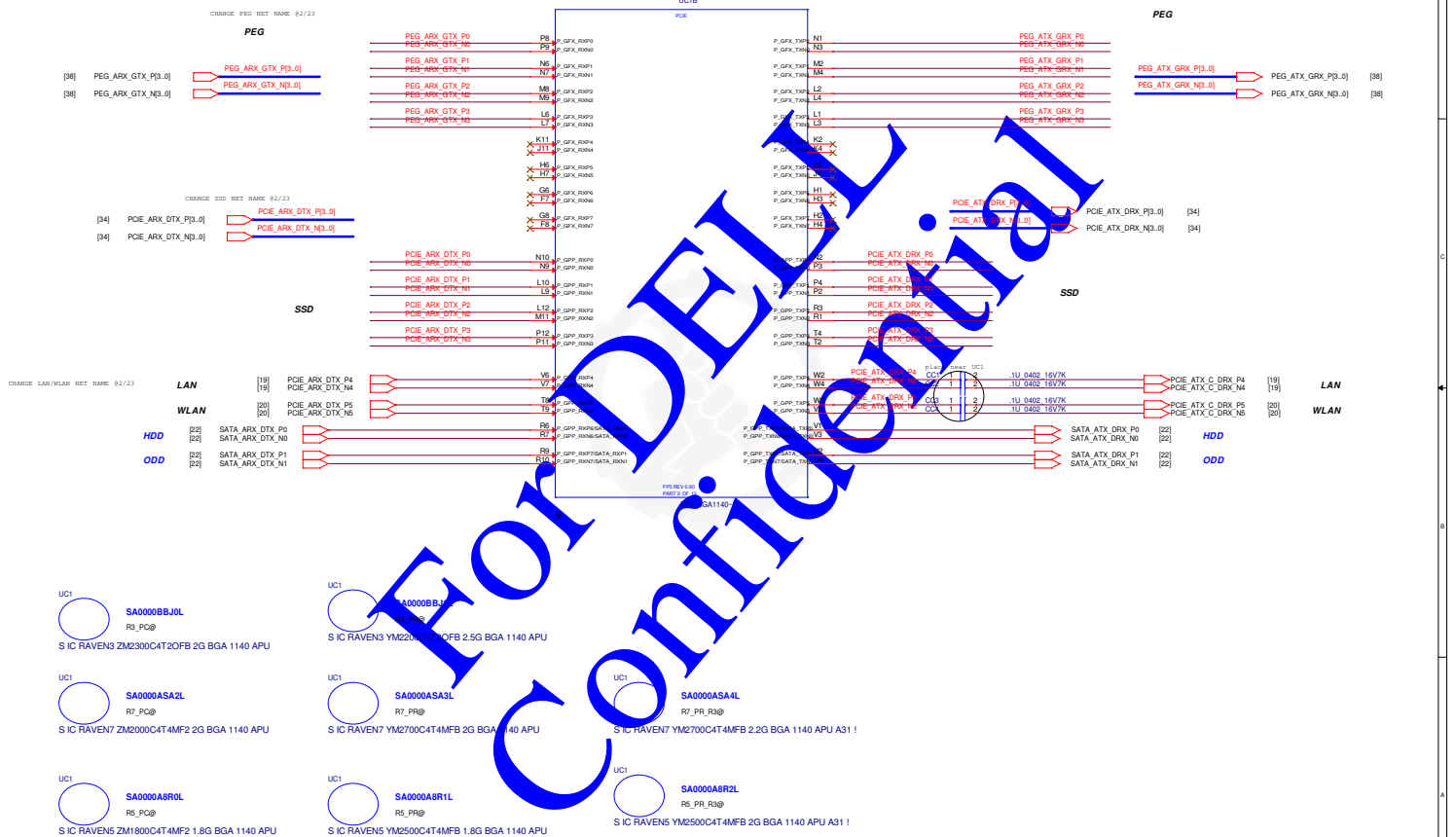


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				Date	Issued
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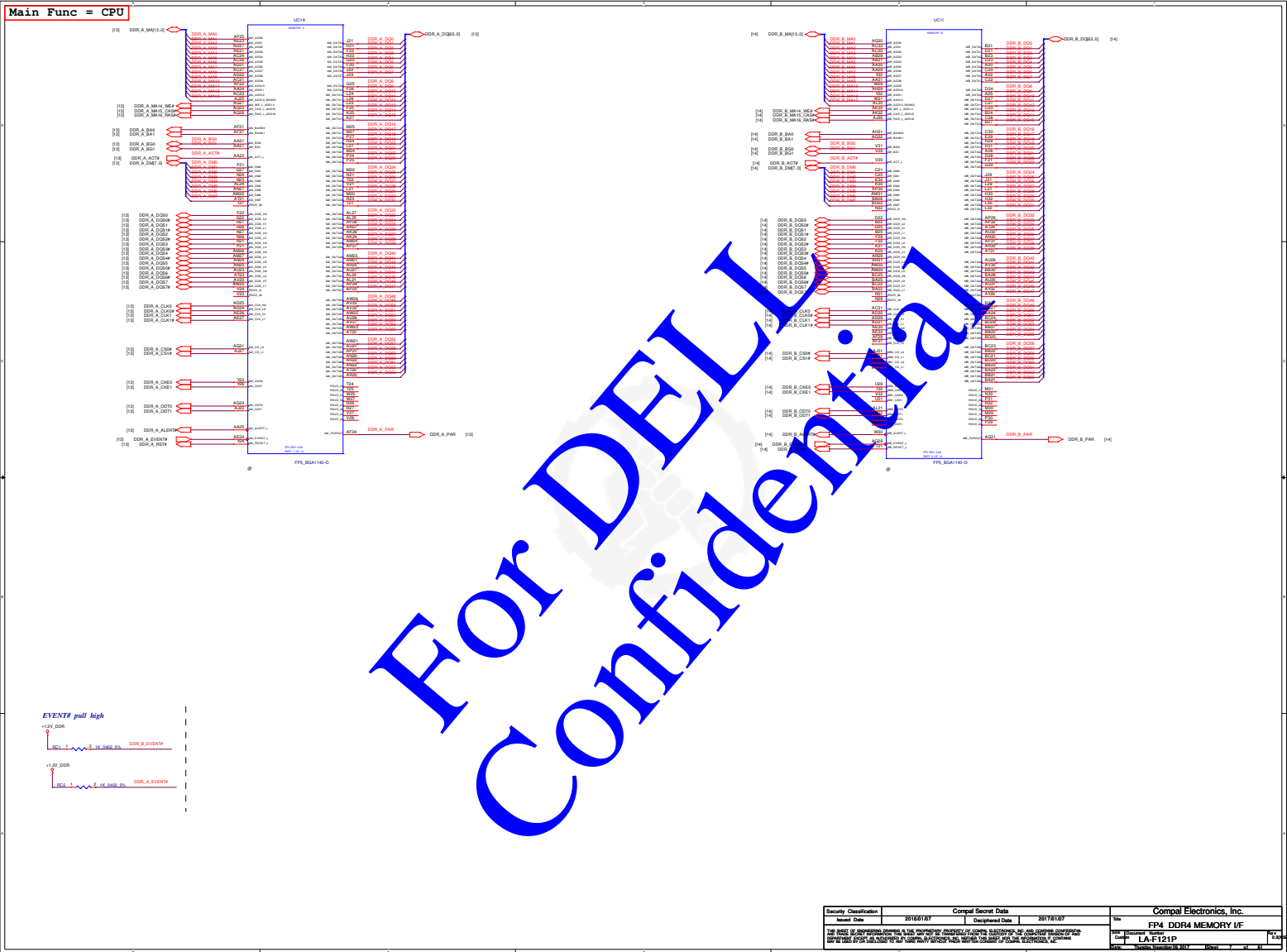
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Main Func = CPU

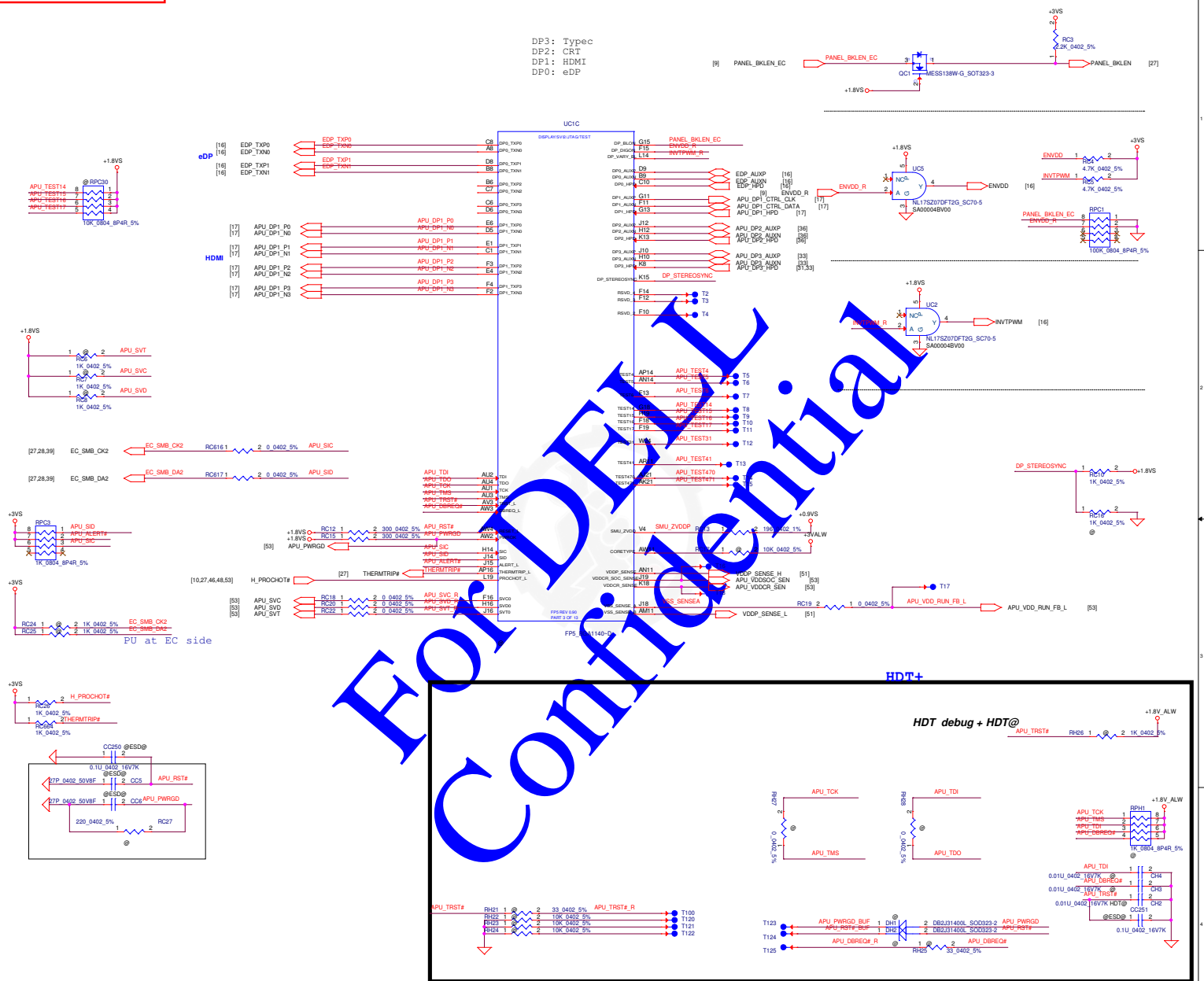


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				Document Number LA-F121P
				Rev 0.30/020
				Date: Thursday, November 09, 2017 18:58:06 6 of 61



Main Func = CPU

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DP3: TypeC
DP2: CRT
DP1: HDMI
DP0: eDP
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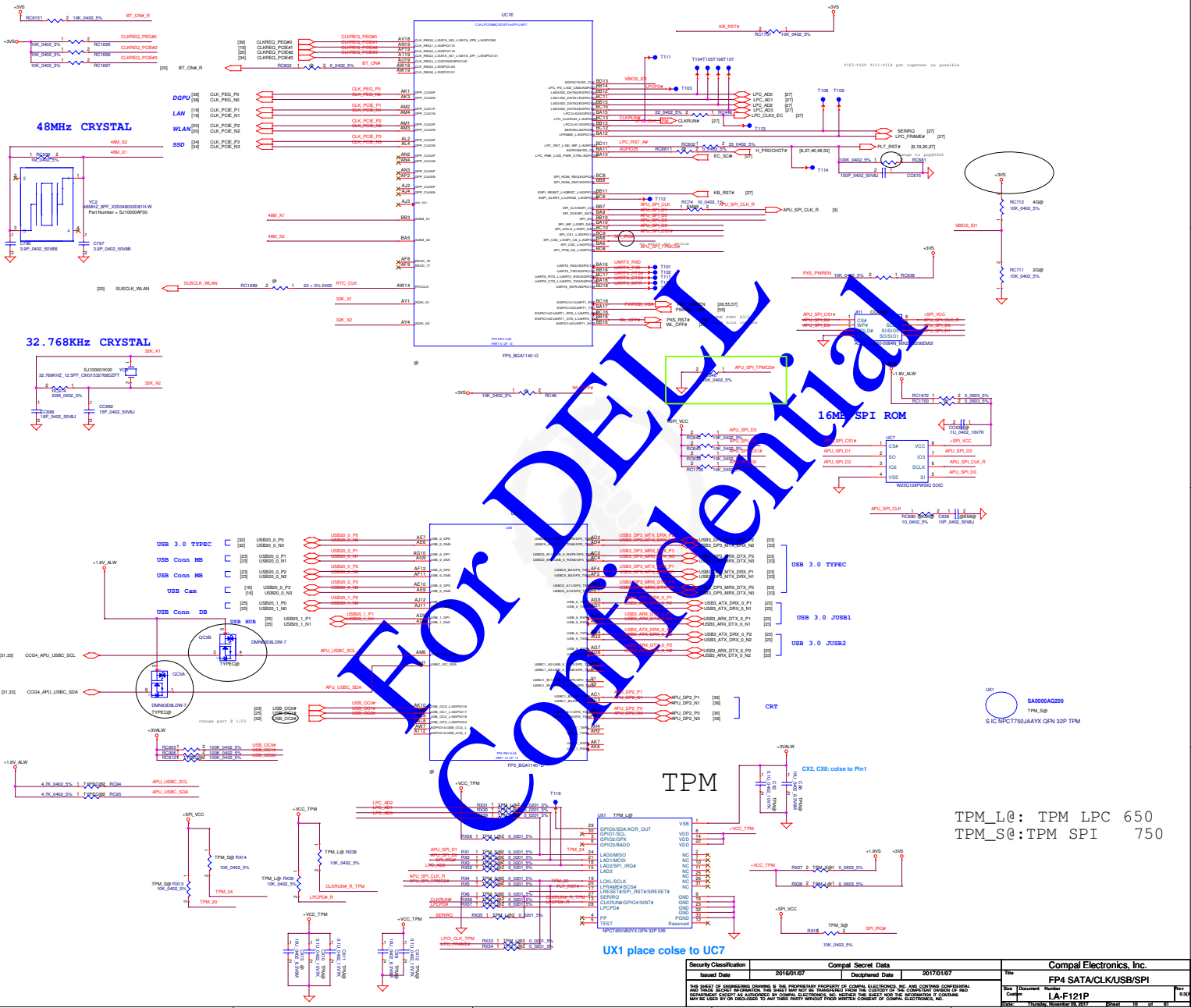


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for Modern standby
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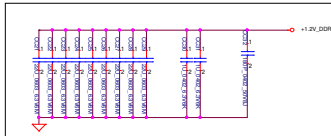
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Main Func = CPU

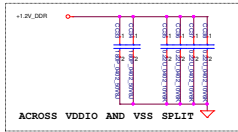


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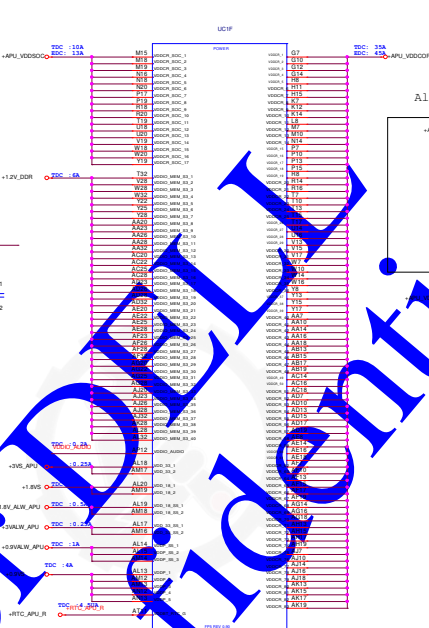
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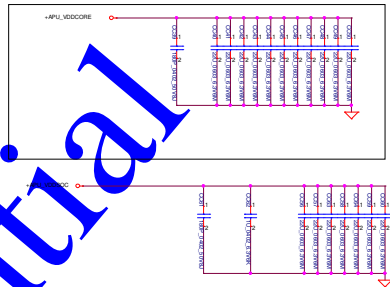
All BU(on bottom side under SOC)



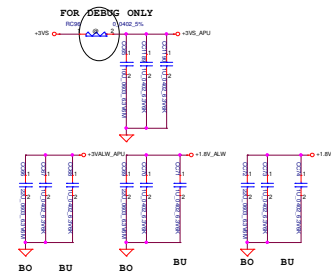
ACROSS VDDIO AND VSS SPLIT



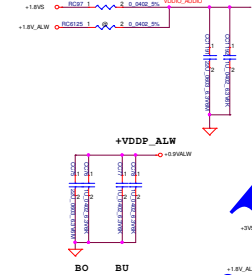
All BU(on bottom side under SOC)



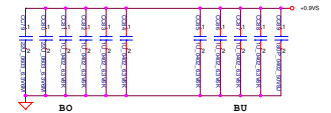
+APU_VDDCORE



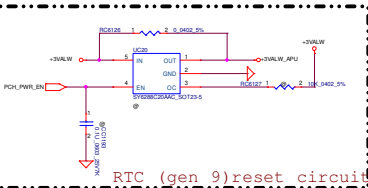
BO BU BO BU BO BU



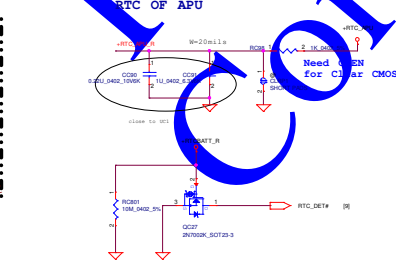
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BO BU

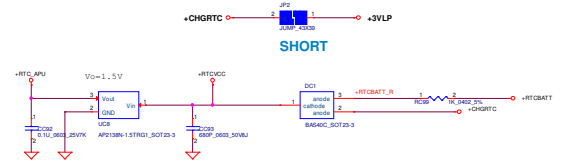


RTC (gen 9)reset circuit



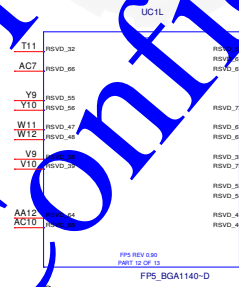
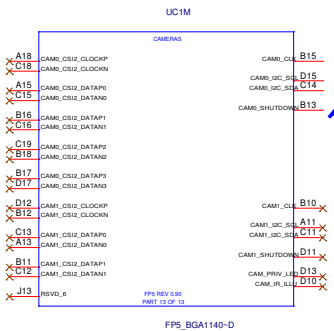
RTC OF APU

Need GEN for Clear CMOS



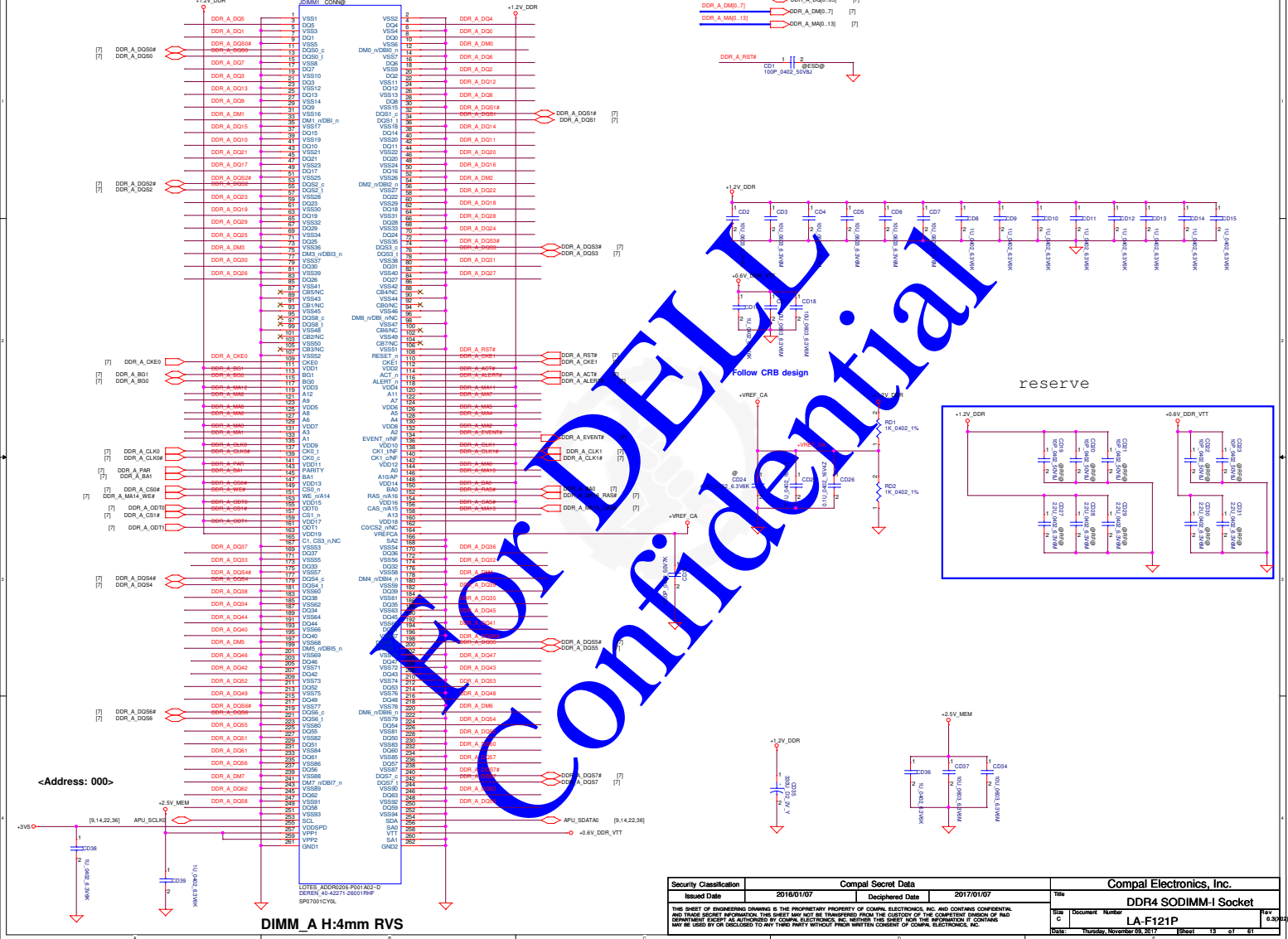
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				Comp	6300
				Rev	1.0



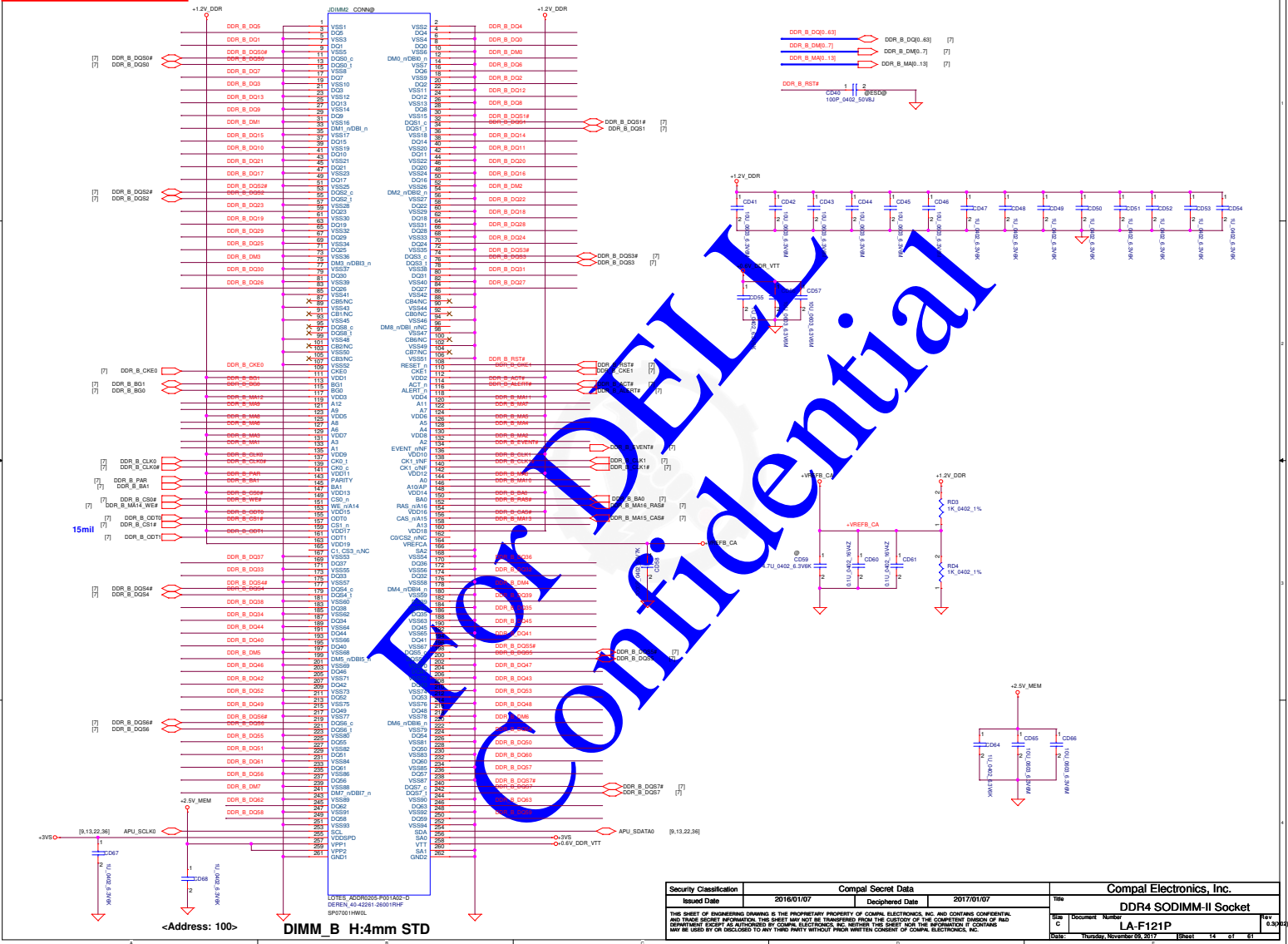
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				Created	Thursday, November 09, 2017	Sheet 12 of 81

Main Func = DIMM1

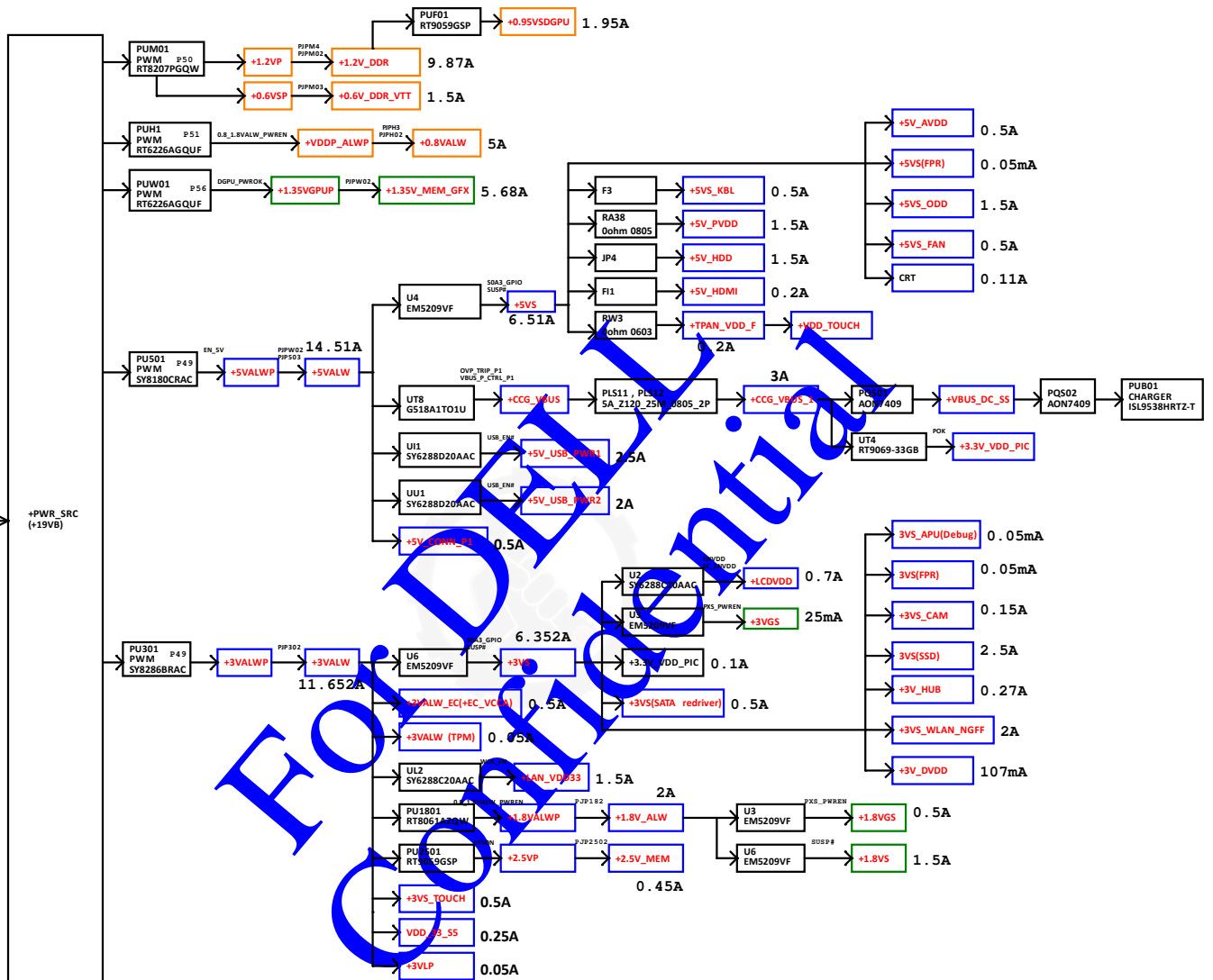
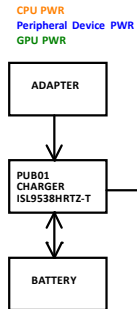


DIMM_A H:4mm RVS

Main Func = DIMM2

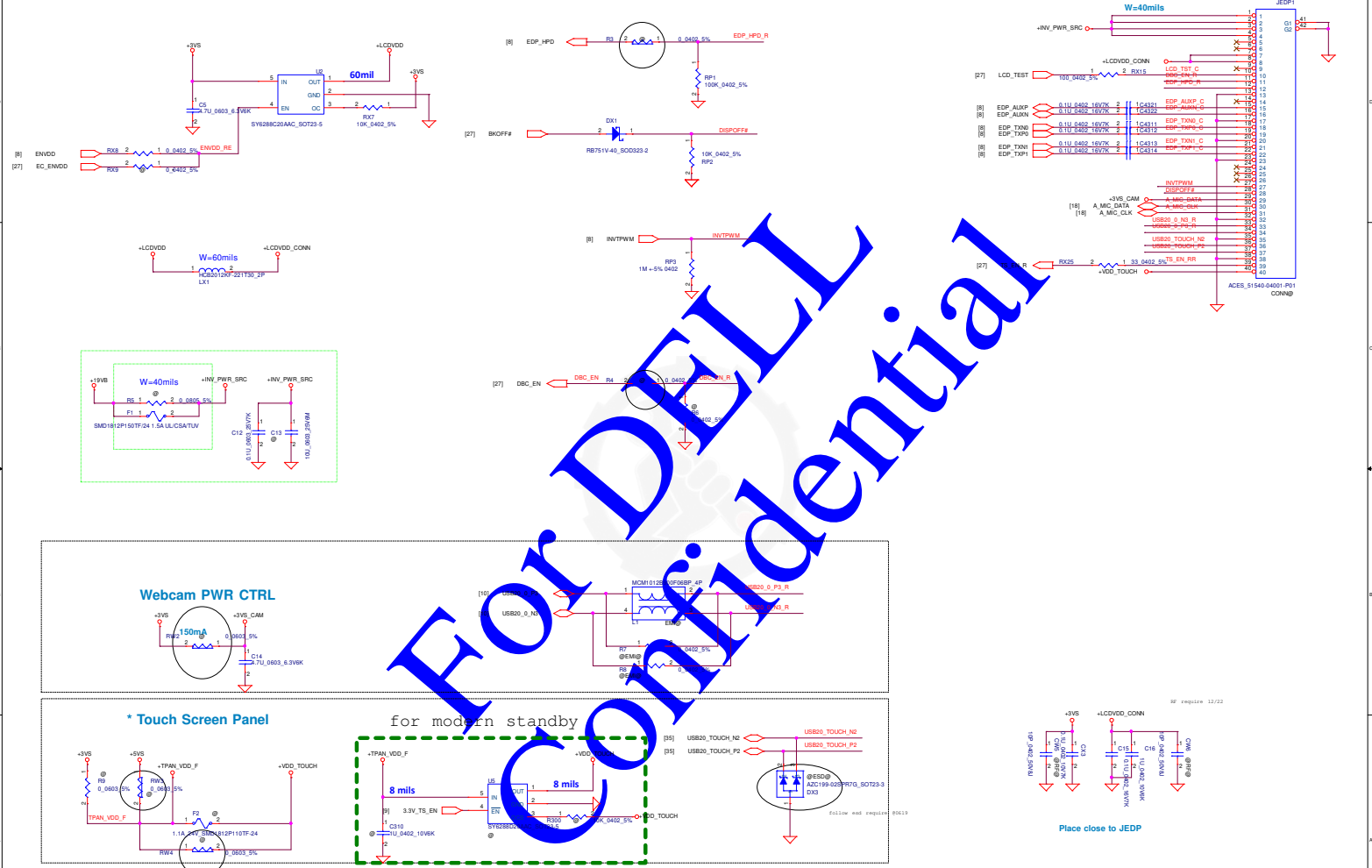


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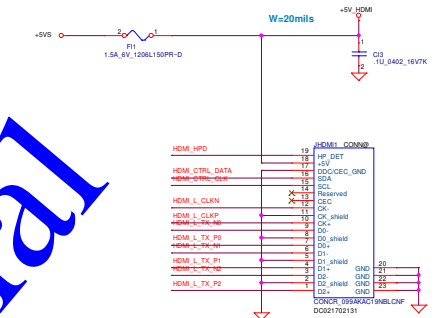
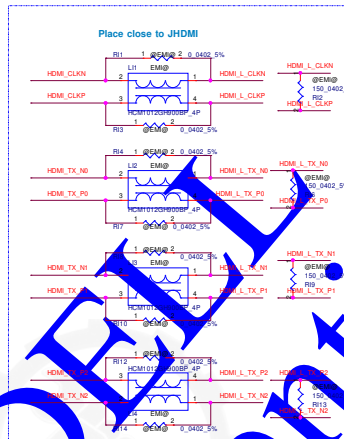
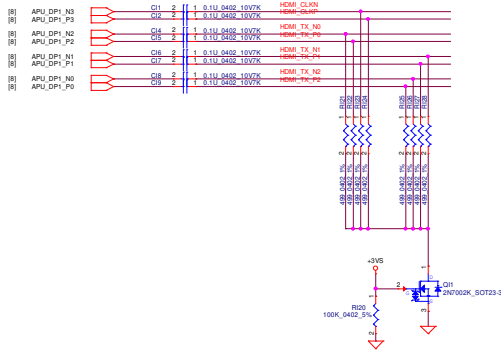
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				LA-F121P
				Rev
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Main Func = LCD

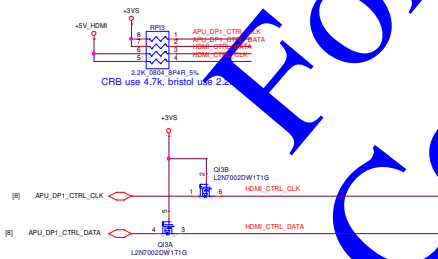


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Main Func = HDMI



Rev	Rev	Rev
1.0	1.0	1.0
1.0	1.0	1.0



Security Classification	Compal Secret Data	Deciphered Date	2017/01/07	2017/01/07	2017/01/07	2017/01/07
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HDMI						
LA-F121P						
Date: December 09, 2017 Sheet: 17 of 61						

Layout Note:
Place close to Pin 13

To eDP

LA5, CA37, CA38 close UAL

A_MIC_CLK A_MIC_DATA LA10 EMIO BLM15B221SN1D 33 6402 5%

[16] A_MIC_CLK
[16] A_MIC_DATA

RAS5

Note: CA9, CA46 close to UAI pin1

Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

EC BEEP

MCU BEEP

PC BEEP

APU_SVR

BEEP

BAT54C SOT23

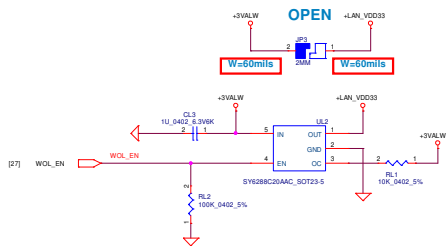
change part: SC28AT347L 04/18

Place on the moat between GND & GNDA.

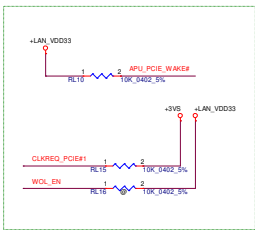
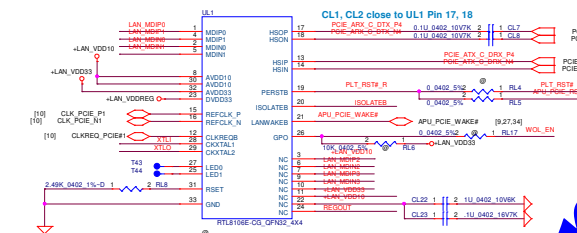
[illegible]

Main Func = LAN

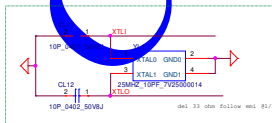
+LAN_VDD33 rising time(10%~90%) : >0.5ms and <100ms



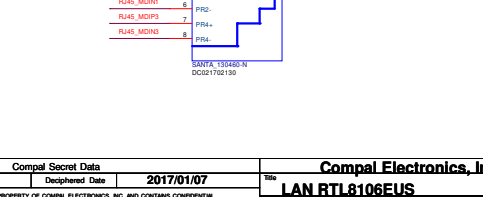
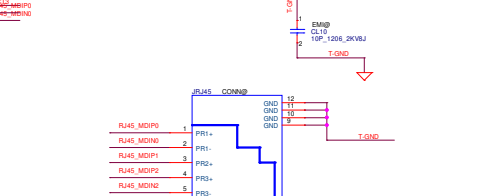
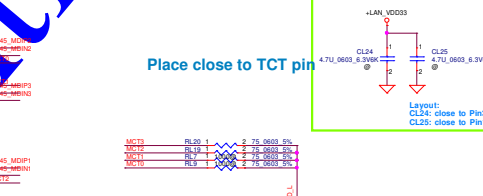
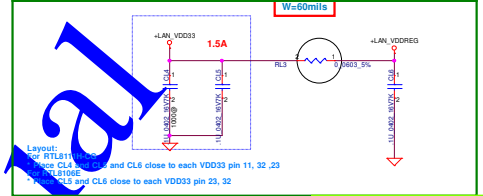
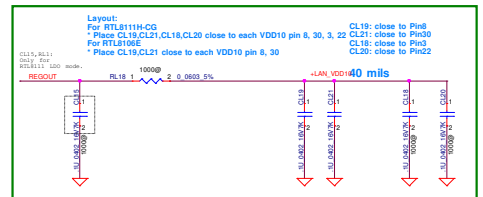
LAN power Noise +LAN_VDD33 < 200mV Vpeak to Vpeak.
LAN power Noise +LAN_VDD10 < 100mV Vpeak to Vpeak.



Reserve 10K pull LAN_IO



XTAL



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Main Func = WLAN

CHANGE WLAN NET NAME 82/23

NGFF WL Con (A Key)

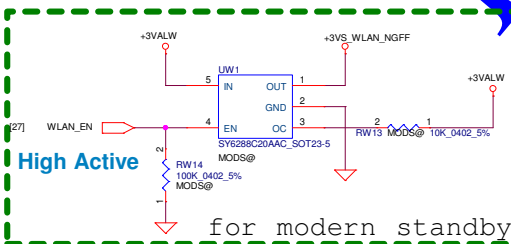
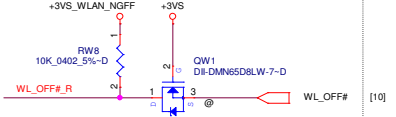
closed to pin 2, 4

+3VS_WLAN_NGFF

+3VS TO +3VS_WLAN_NGFF

+3VS 1 2 0.1206, 5% +3VS_WLAN_NGFF

Prevent Backdriver from +3VS_WLAN_NGFF to +3VS



Security Classification

Compal Secret Data

Issued Date

2016/01/07

Deciphered Date

2017/01/07

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Compal Electronics, Inc.

Title

NGFF WLAN

Size

Document Number

LA-FI21P

Date

Thursday, November 09, 2017

Sheet

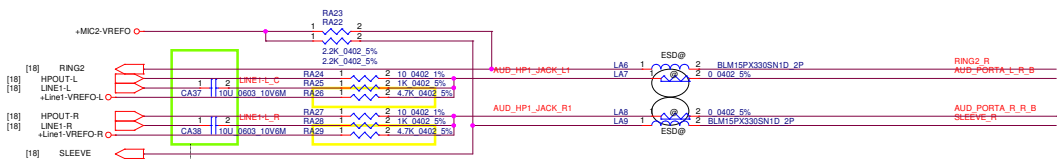
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of

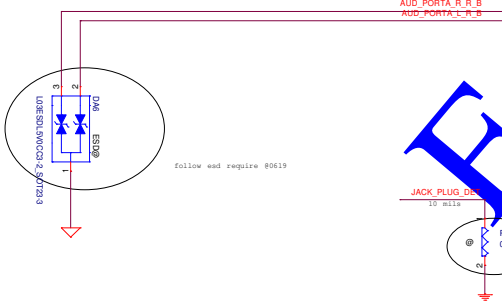
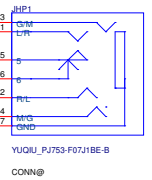
61

Rev

030402

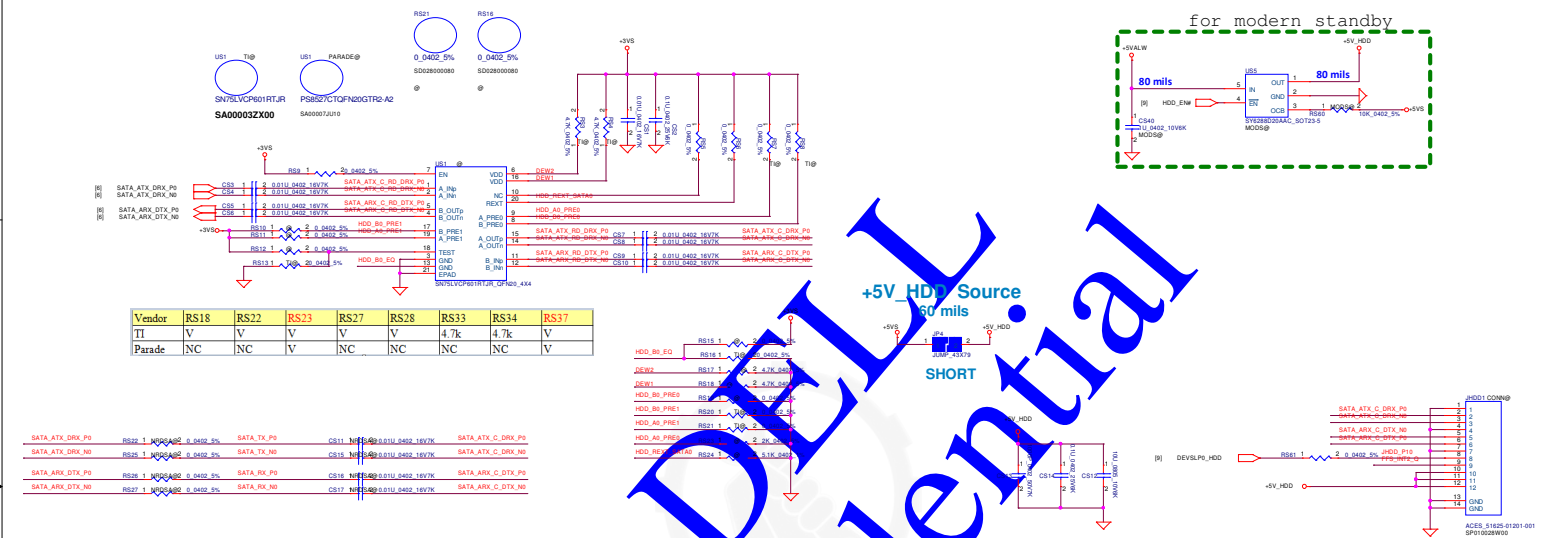
Main Func = Audio Jack

CLOSE TO JHP

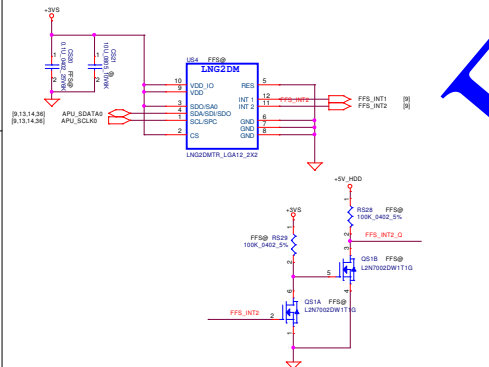
Universal Jack
(Global Headset Jack + mic phone in + line in support)

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Date: Thursday, November 09, 2017				Sheet 21 of 61

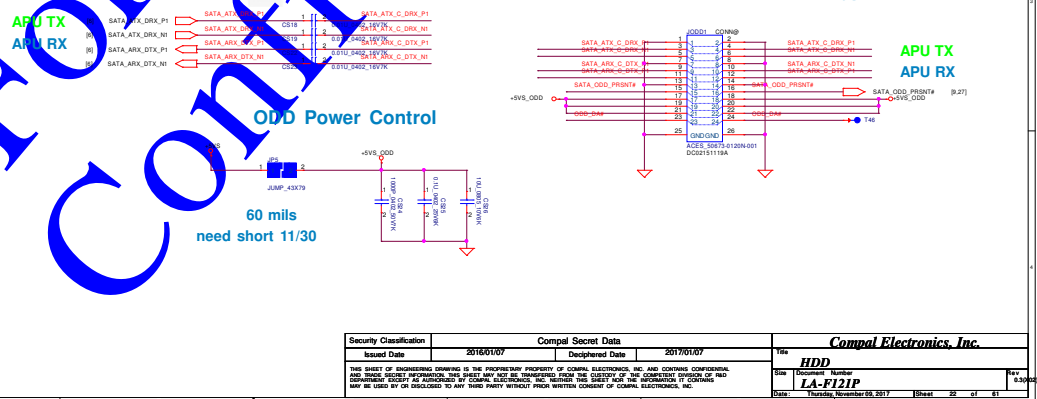
Main Func = HDD



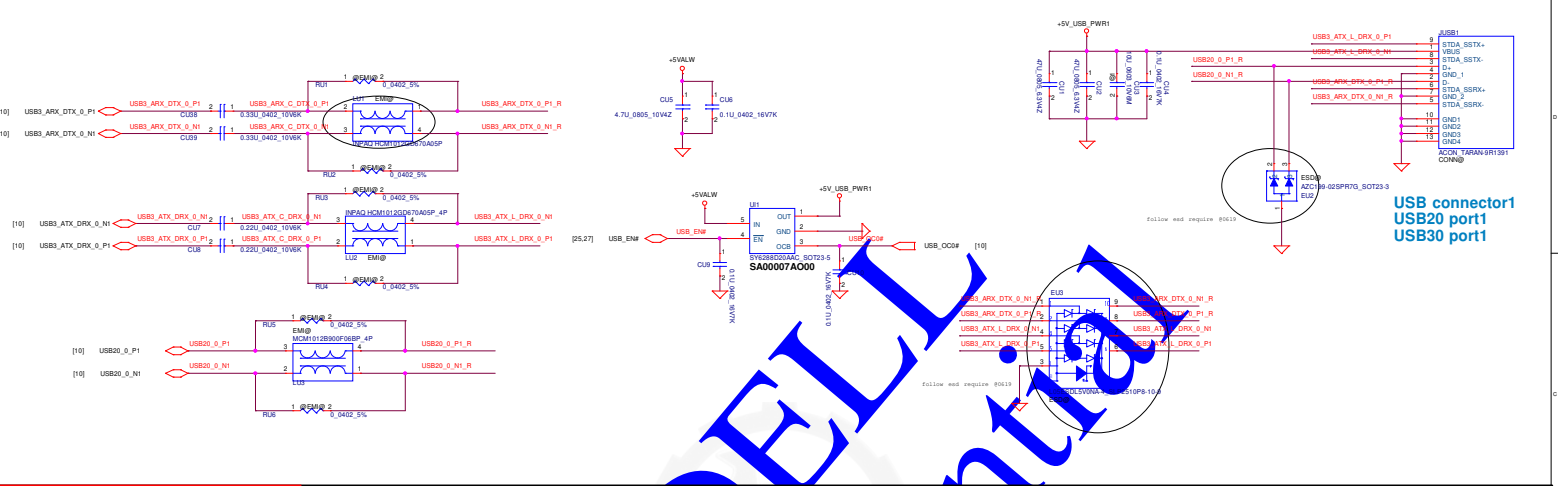
Main Func = FFS



Main Func = ODD



Main Func = USB3.0 Port1

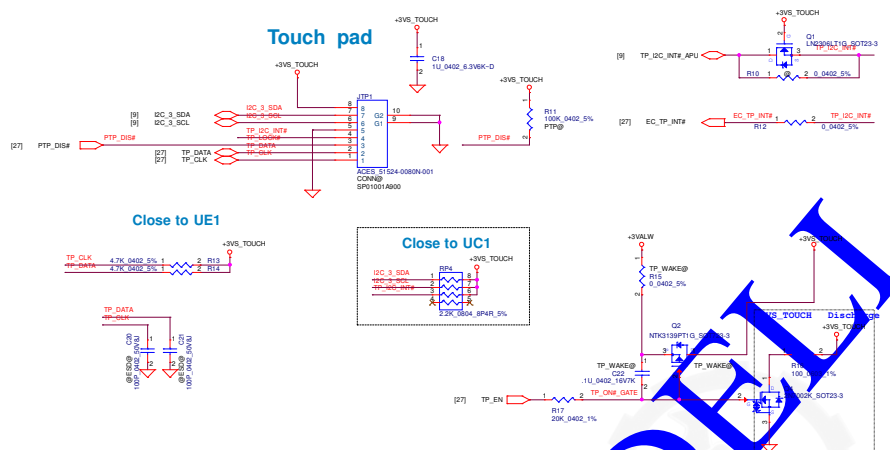


Main Func = USB3.0 Port2

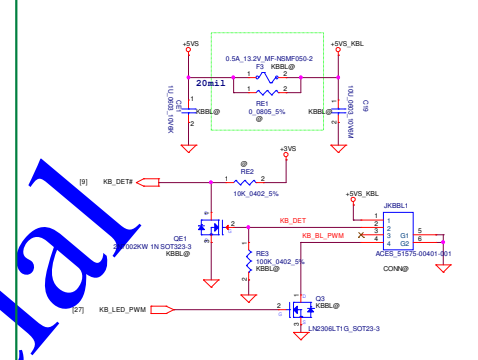


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				Doc Name	LA-F121P
				Rev.	1.0
				Rev.	1.0

Main Func = Touch Pad

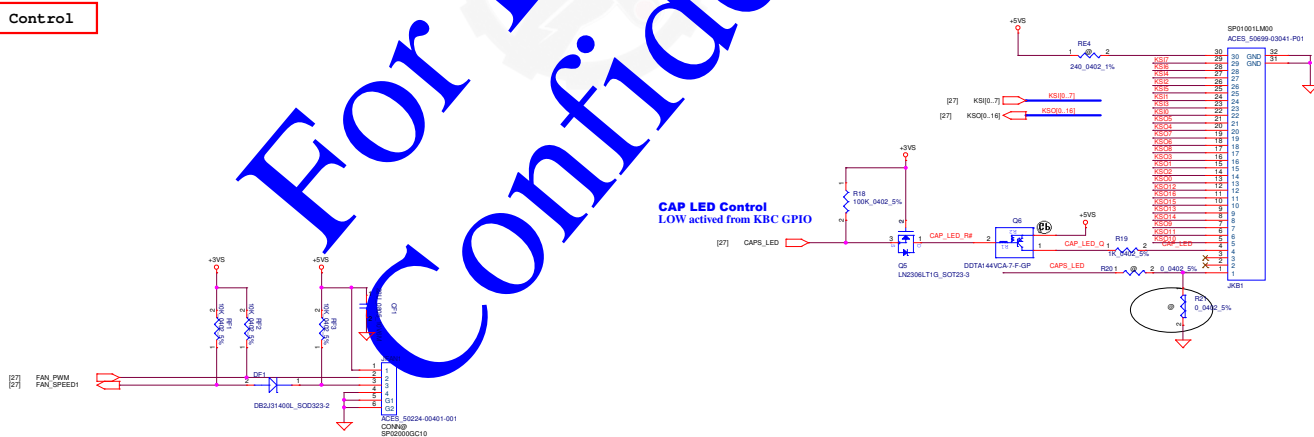


Main Func = KBBL

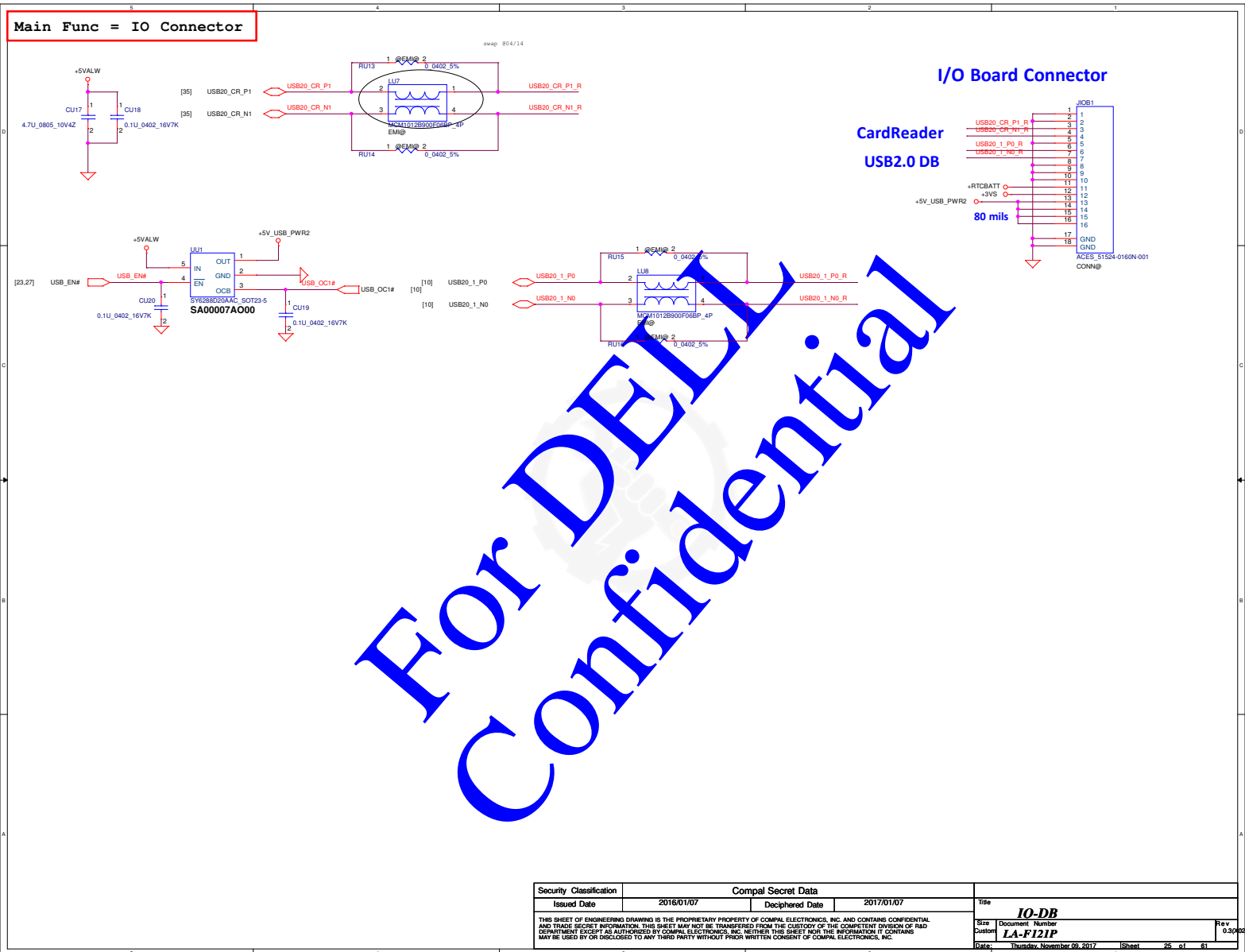


Main Func = KB

CAP LED Control
LOW acted from KBC GPIO

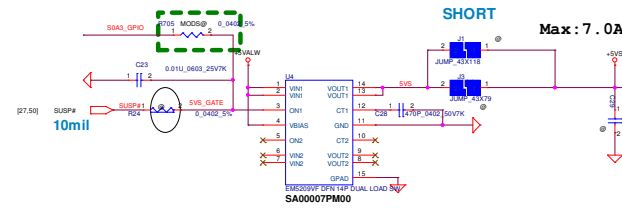


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				1A-F121P	
				Date: Thursday, November 08, 2017 Sheet: 24 of 61	

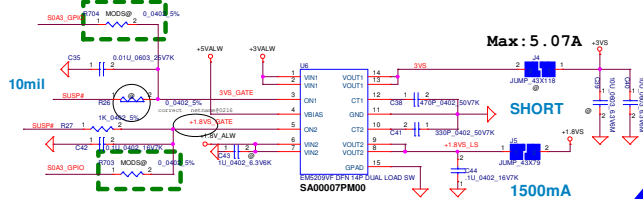
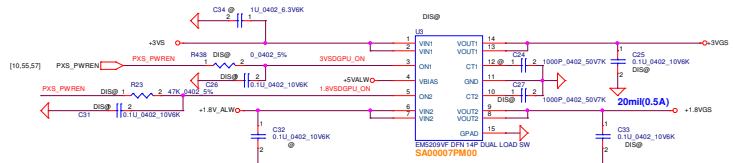


Main Func = DC Interface

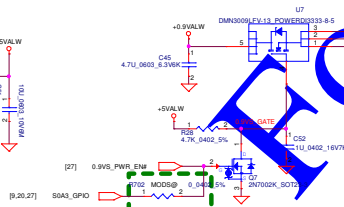
+5VS and +3VS switch




+3VS to +3VGS
+1.8V_ALW to +1.8VGS



Max: 4A



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				LA-F121P
				Date: Thursday, November 09, 2017 10:58:28 AM 8.31M

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			EC EN- KB90124/4/KB90220C	Rev
			LA-F121P	0.01
			Date	Thursday, November 09, 2017 10:01am 27 of 61

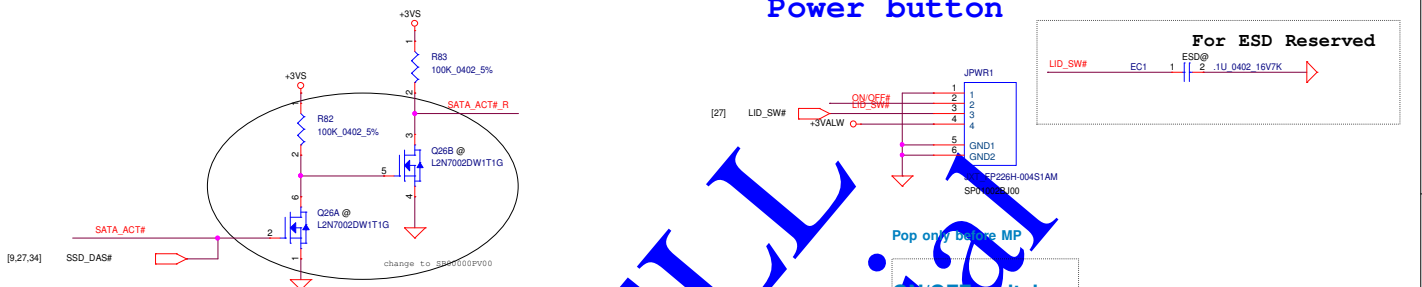
Main Func = Thermal Sensor

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Size				Document Number
Date				LA-F121P
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Main Func = POWER BTN

Power button

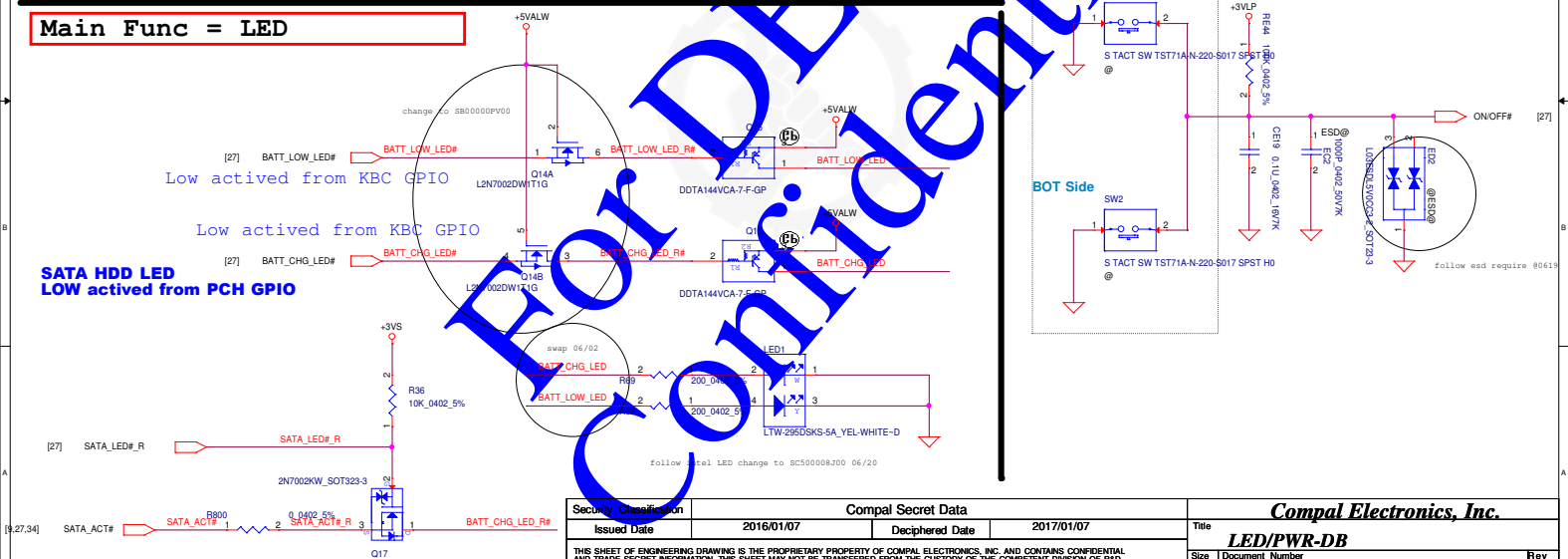
For ESD Reserved



Main Func = LED

Pop only before MP
ON/OFF switch
TOP Side

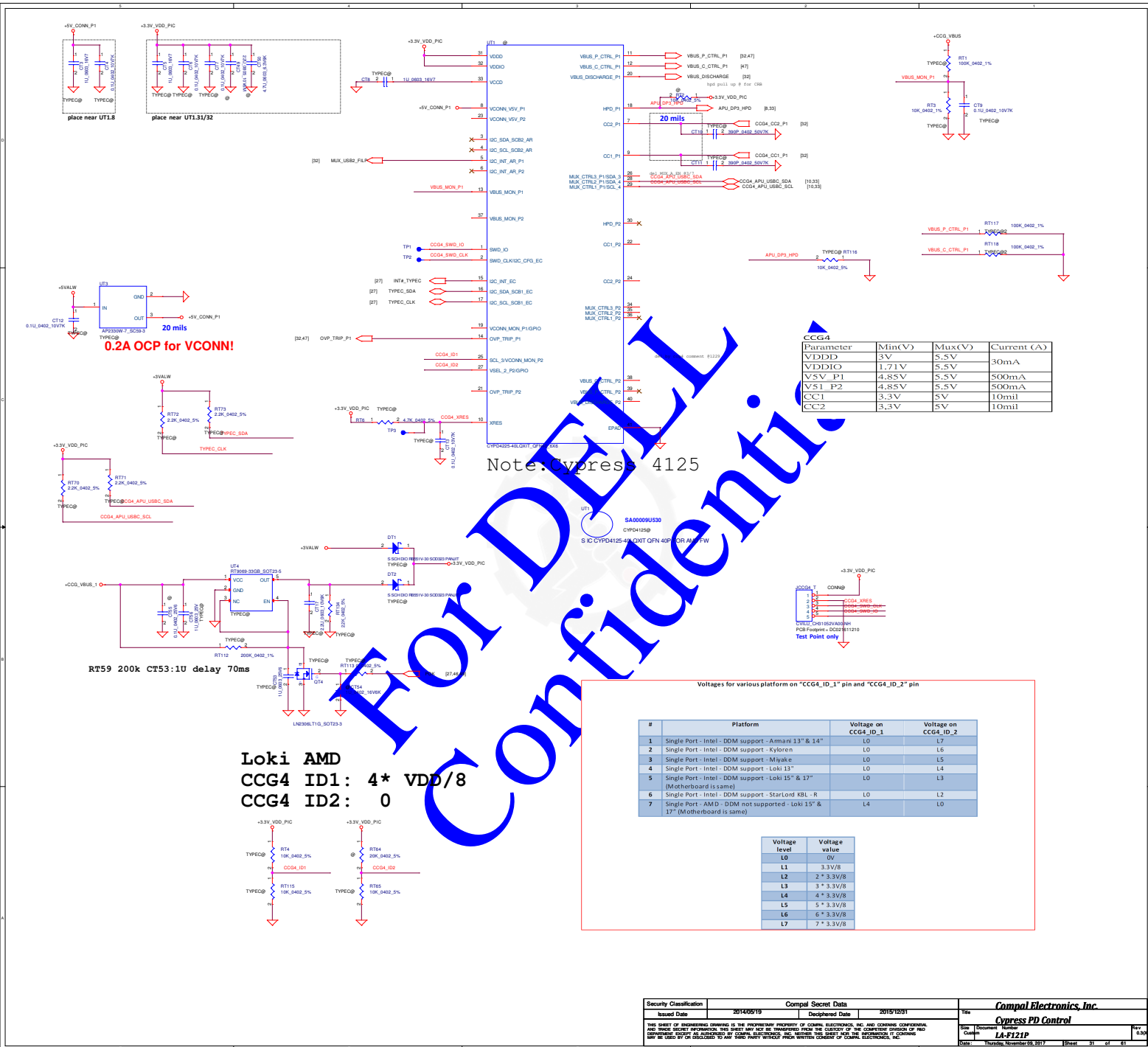
BOT Side



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		LED/PWR-DB	
2016/01/07		2017/01/07		Size	
				Document Number	
				LA-F121P	
				Date	
				Thursday, November 09, 2017	
				Sheet	
				29 of 61	

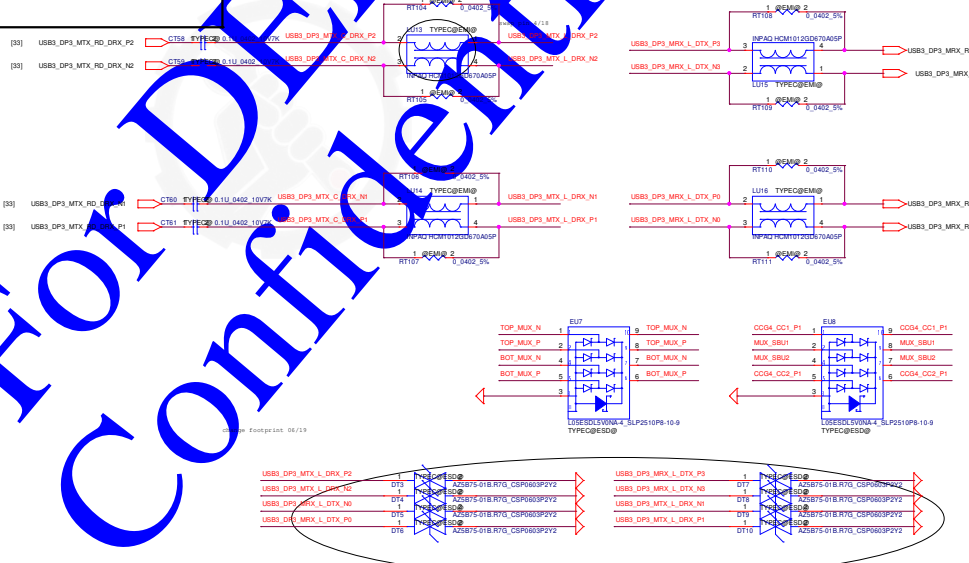
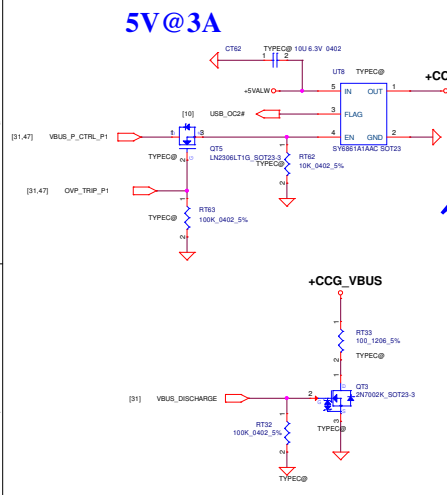
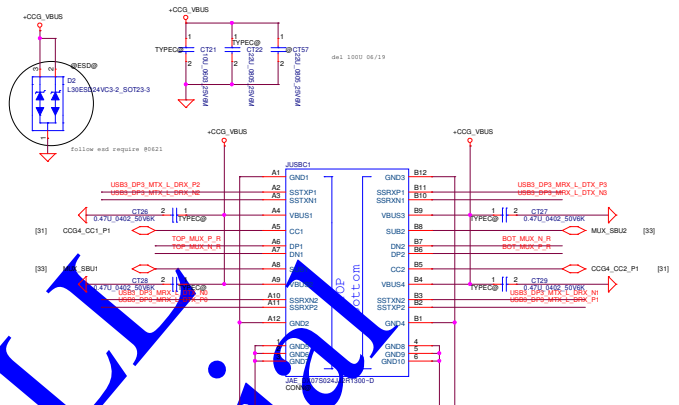
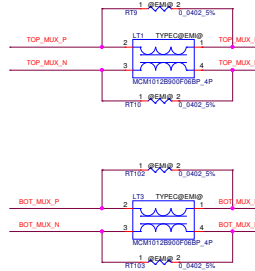
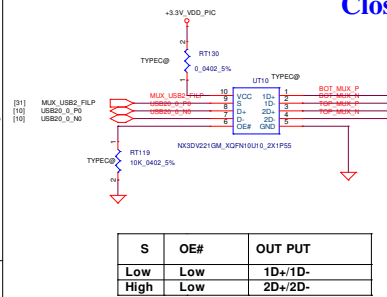
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LED/PWR-DB
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0.3/02



Main Func = USB2 Mux

Close to JUSBC1 <500mil



Type-C 5V Provide Path Control

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Rev		C		1	
Date		2014/05/19		1	

The schematic diagram illustrates the USB3.0 PHY interface for the T505044-0 1/25. It shows the connection between the USB3.0 PHY (T505044-0) and the T505044-0 1/25. The diagram includes signals for TX, RX, and control lines, along with power and ground connections. A large blue diagonal watermark 'For Confidential' is overlaid on the diagram.

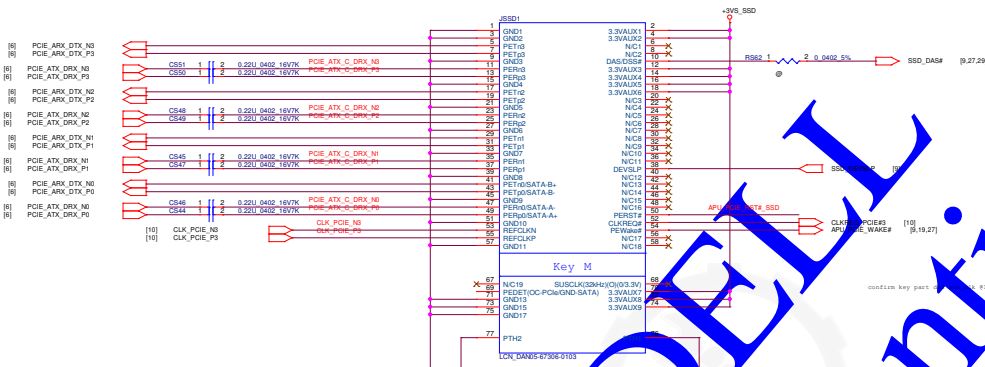
Legend:

- TX_C, RD, DTX_P2
- TX_C, RD, DTX_P1
- TX_C, RD, DTX_P0
- TX_C, RD, DTX_P3
- TX_C, RD, DTX_P4
- TX_C, RD, DTX_P5
- TX_C, RD, DTX_P6
- TX_C, RD, DTX_P7
- TX_C, RD, DTX_P8
- TX_C, RD, DTX_P9
- TX_C, RD, DTX_P10
- TX_C, RD, DTX_P11
- TX_C, RD, DTX_P12
- TX_C, RD, DTX_P13
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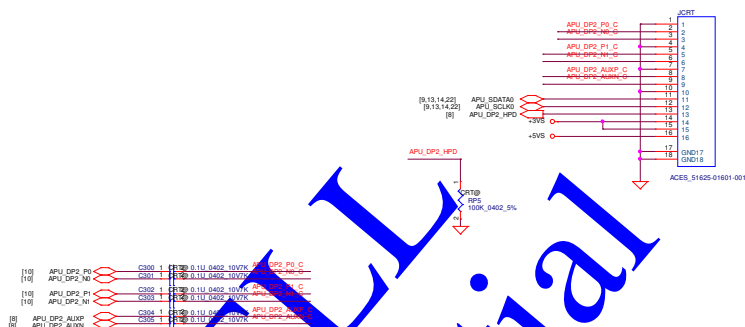
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			Drawn Checked Date 2017/05/06		01

Main Func = SSD

NGFF Key M

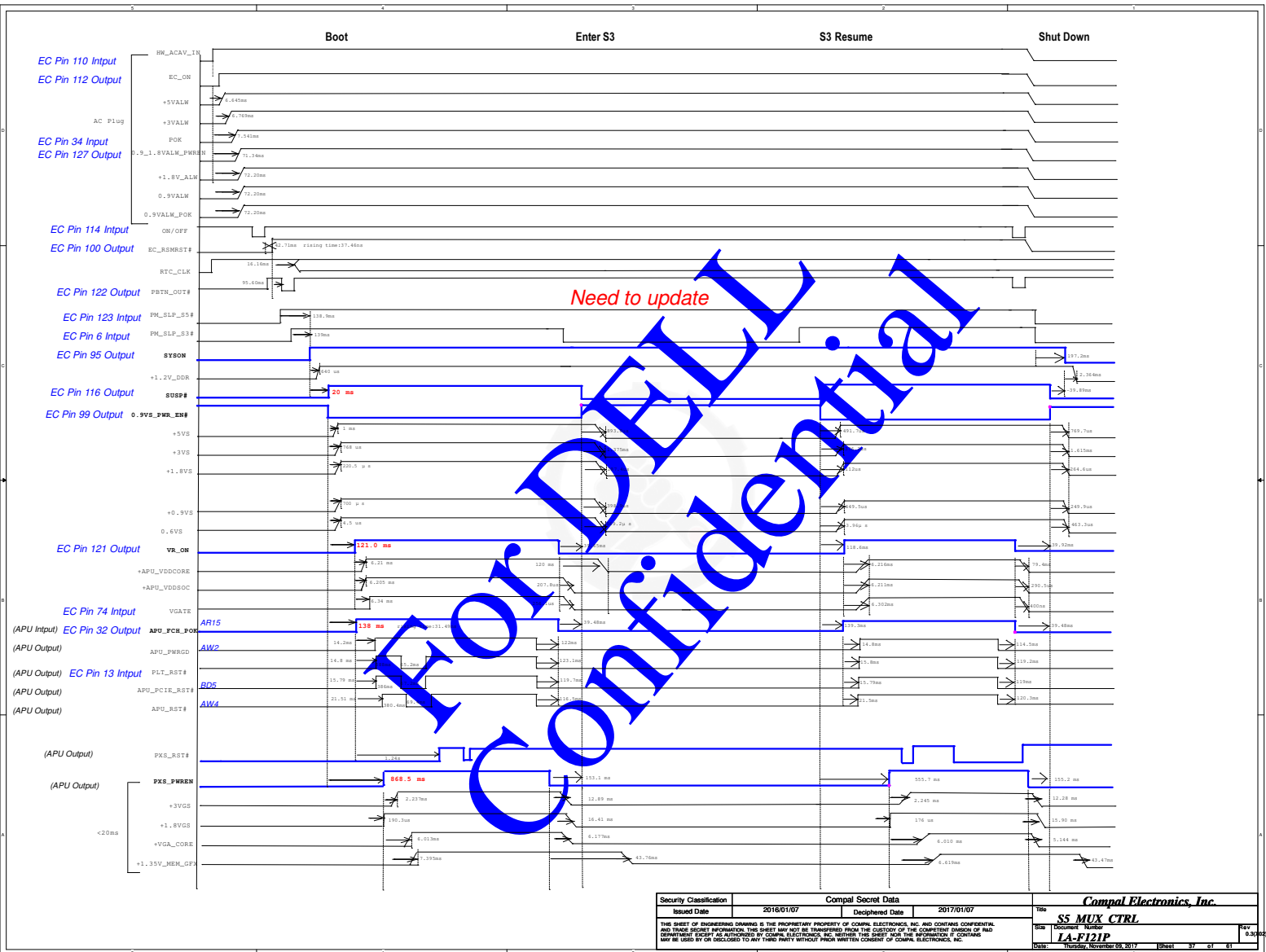


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Doc No.	LA-F121P	Rev	1.00	Doc No.	LA-F121P

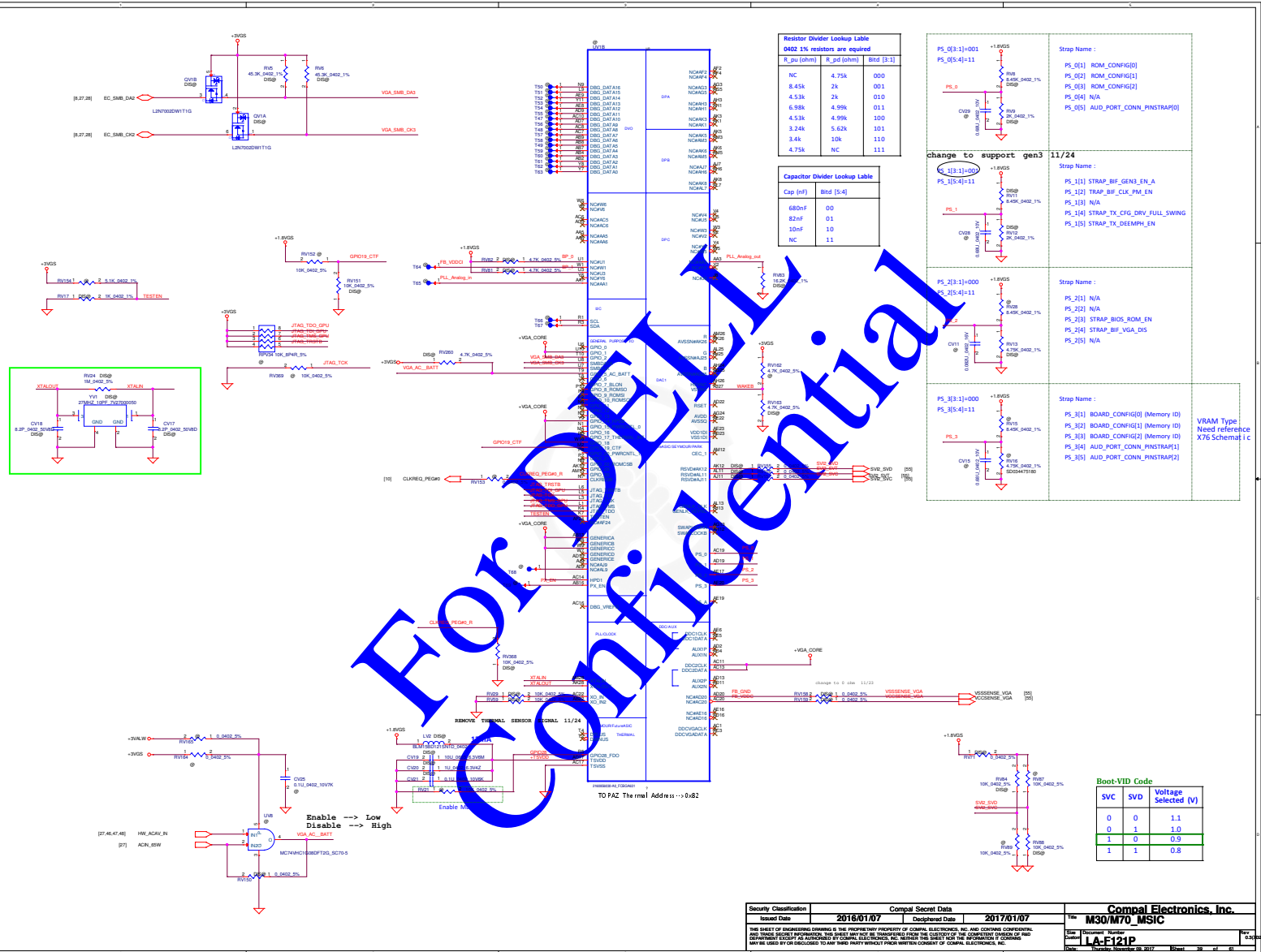


For DELL Confidential

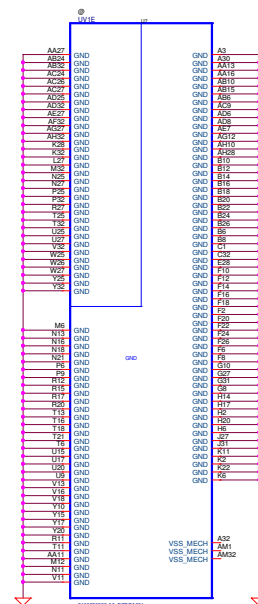
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				Serial Number	
				LA-FLIIP	
				Date:	
				Rev	B.306







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				Rev	LA-E121P



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Date	Document Number	Revision	40	41	42

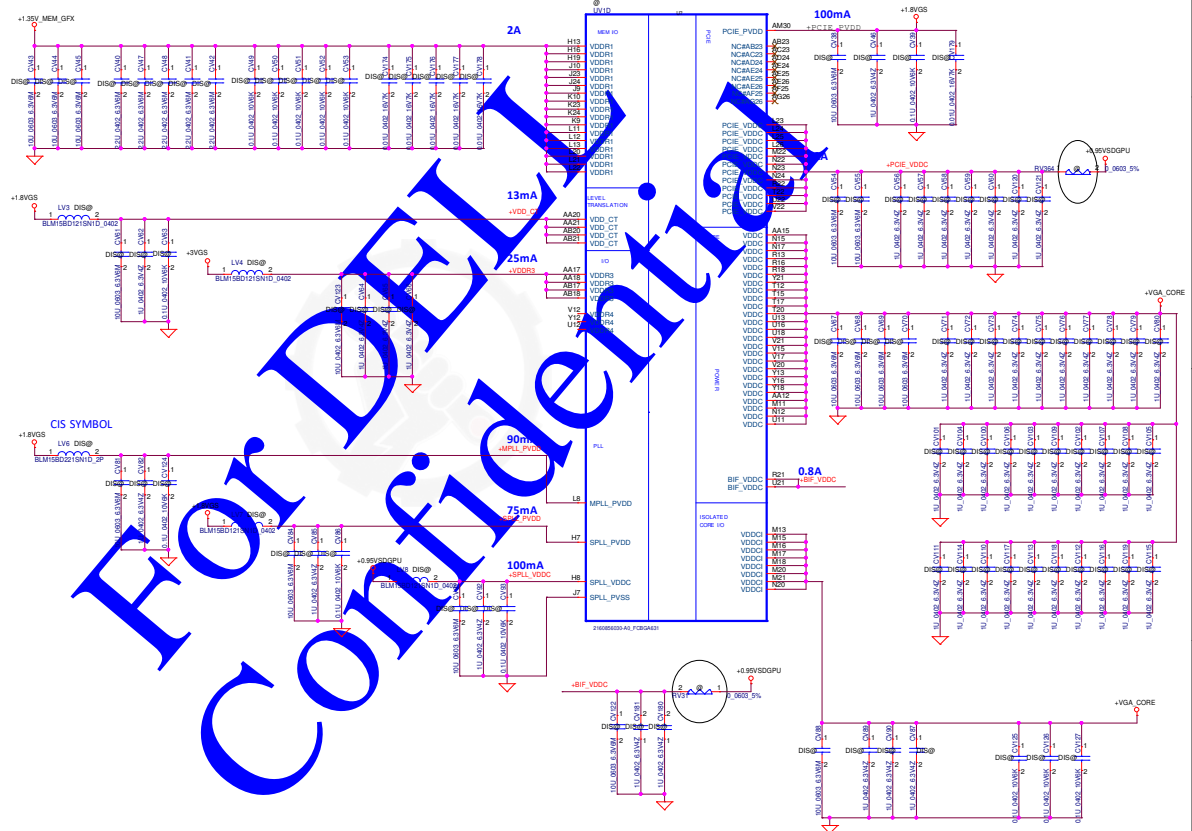
+VGA_CORE	10uF	1uF	0.1uF
VDDC	4	30	0
VDDCI	1	3	3

+0.95VSDGPU	10uF	1uF	0.1uF
PCIE_VDDC	2A	2	7
BIF_VDDC	0.8A	1	2
SPLL_VDDC	100mA	1	1

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1 2A	3	5	5	5

+1.8VGS	10uF	1uF	0.1uF	0.01uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	90mA	1	1	0
SPLL_PVDD	75mA	1	1	0
VDD_CT	13mA	1	1	0
+DP_VDDR	40mA	1(0)	1(0)	1(0)
+DP_VDDC		1(0)	1(0)	1(0)

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	1	3	0



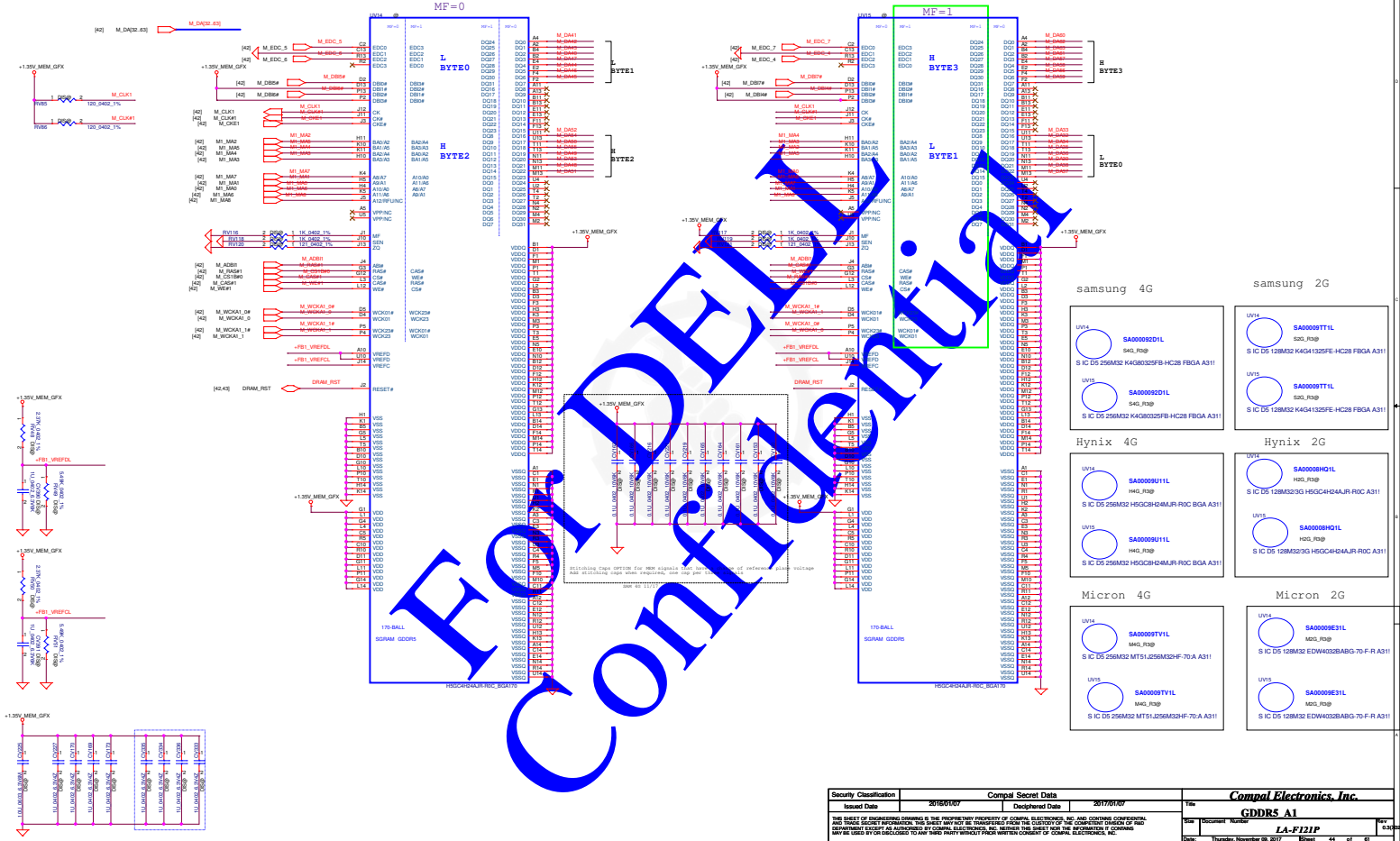
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Issued Date	2016/01/07	Deciphered Date	2017/01/07	
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Rev	Customer	Title		Rev
		M30/M70 Power		0.0009
		LA-F121P		
		Date: Thursday, November 03, 2017		Rev: 01 07 01



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			Date	1-A-E129-20.07	
			Sheet	42 of 61	

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				LA-712121		6.3/2016
				Date	Thursday, November 28, 2017	Time
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clamshell configuration



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			Date	Thursday, November 09, 2017 11:44 AM

Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as 750 mV/ μ s).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.

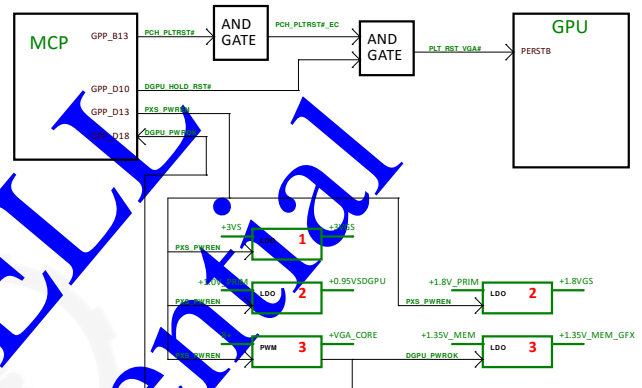
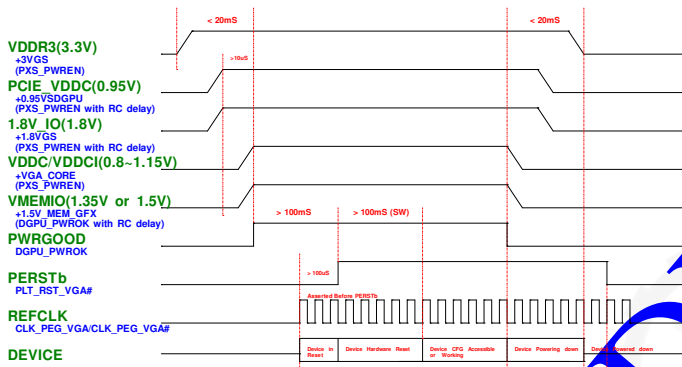


Table 3–21 Resistor Divider Lookup T

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

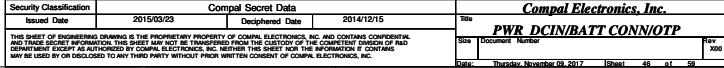
Note: 0402 1% resistors are required.

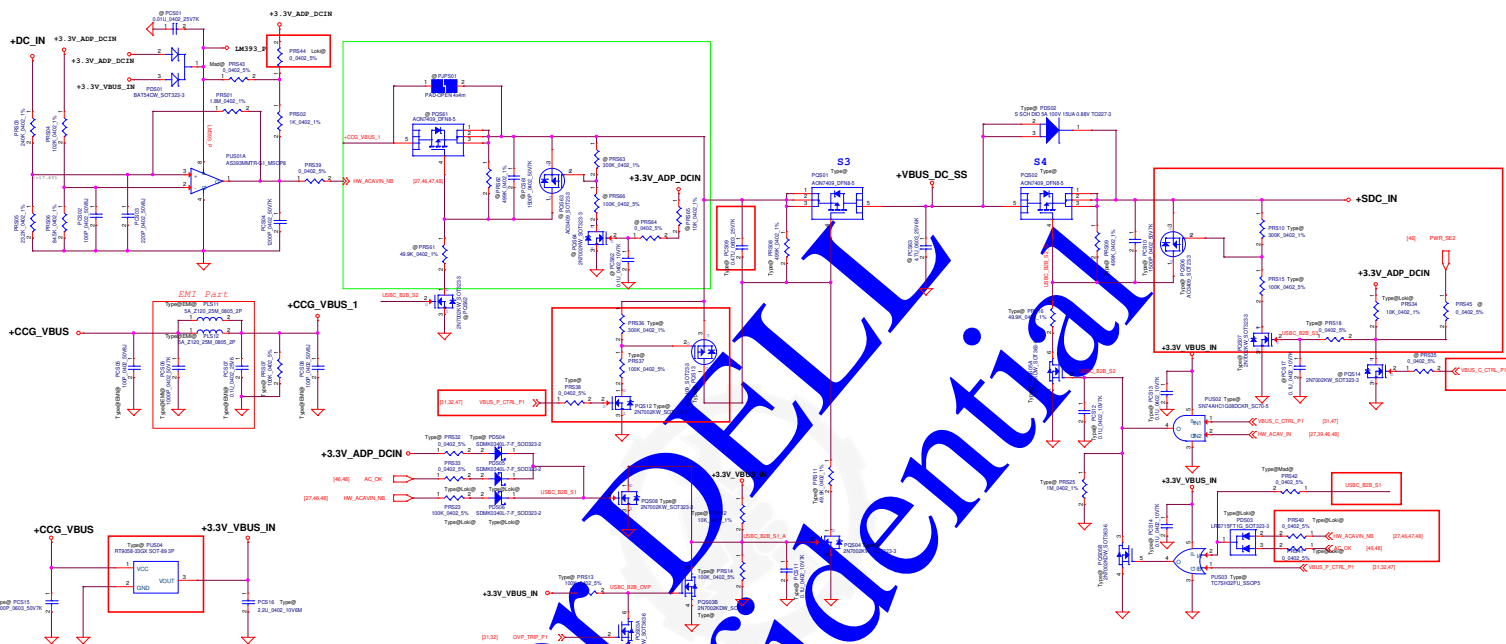
For AMD R17M-M2-50 VRAM Only

Memory ID	R3 P/N	Vendor	Configuration	Size
000	SA00009T1L	SAMSUNG	S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	2GB
110	SA00008HQ1L	Hynix	S IC D5 128M32/3G H5GC4H24JR-R0C A31!	2GB
111	SA00009E31L	Micron	S IC D5 128M32 EDW4032BAG-70-F-R A31!	2GB

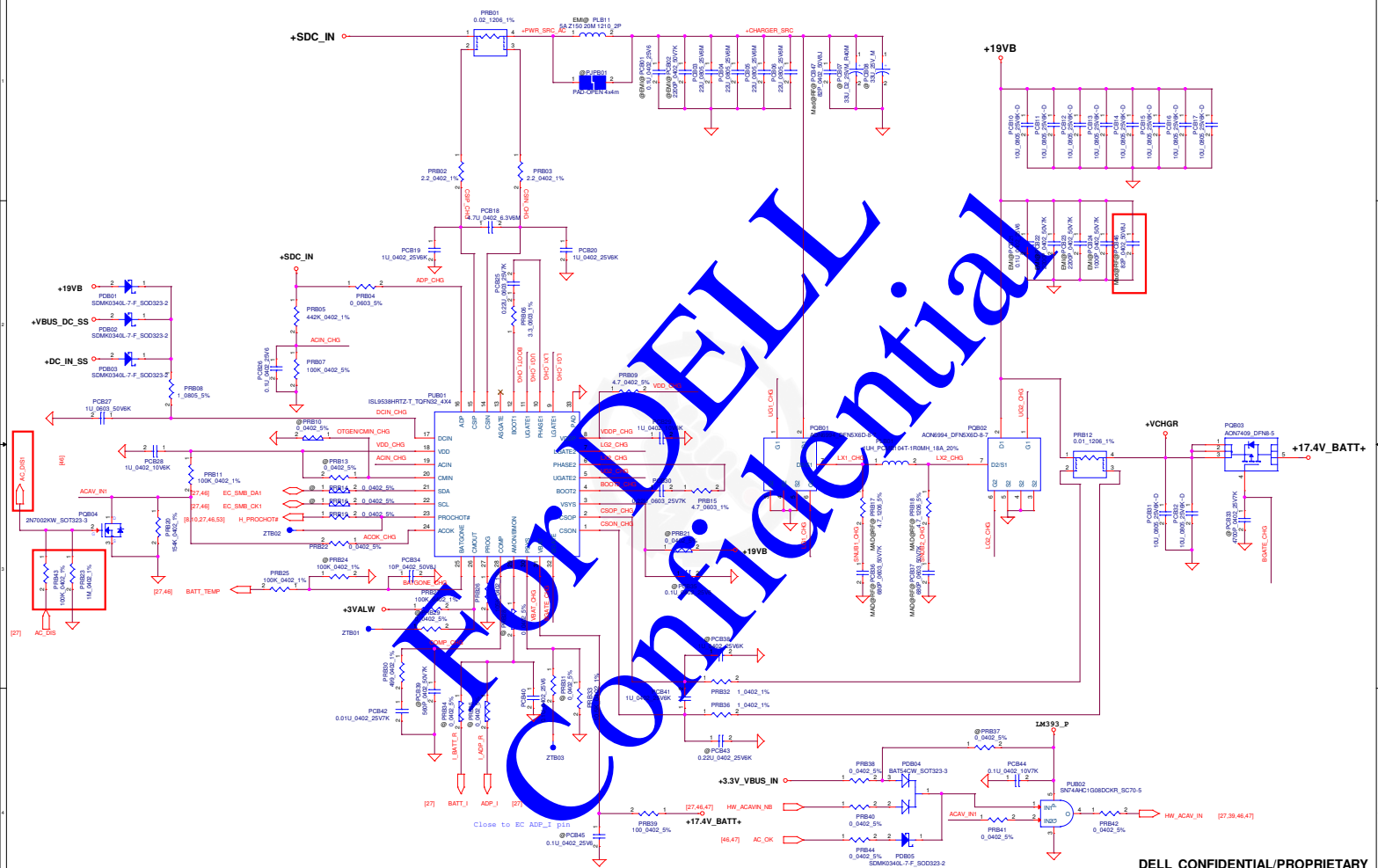
Memory ID	R3 P/N	Vendor	Configuration	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	4GB
110	SA00009U11L	Hynix	S IC D5 256M32 H5GC8H24MR-R0C BGA A31!	4GB
111	SA00009TV1L	Micron	S IC D5 256M32 MT51J256M32HF-70-A A31!	4GB

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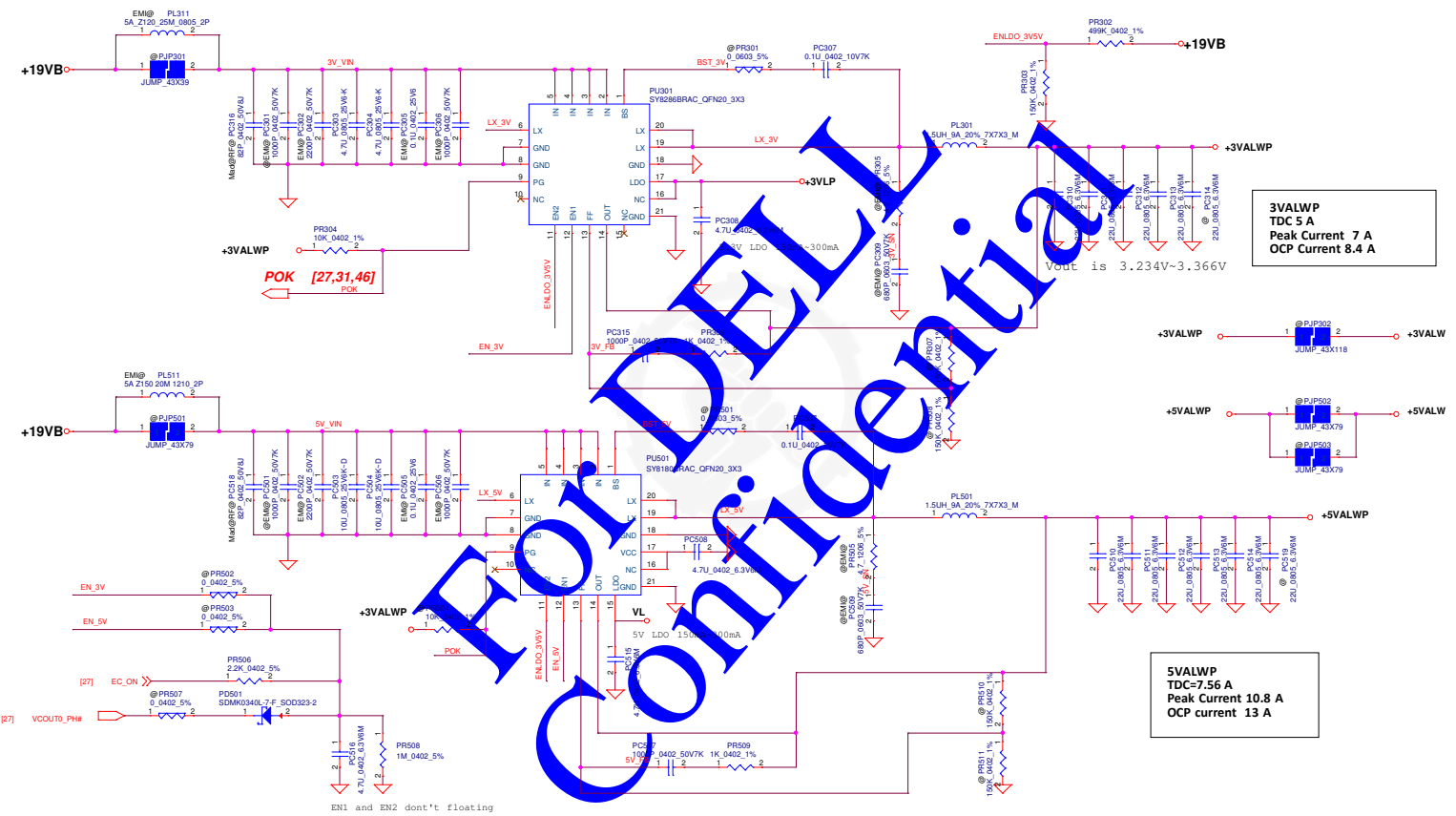
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Main Func = CHARGER



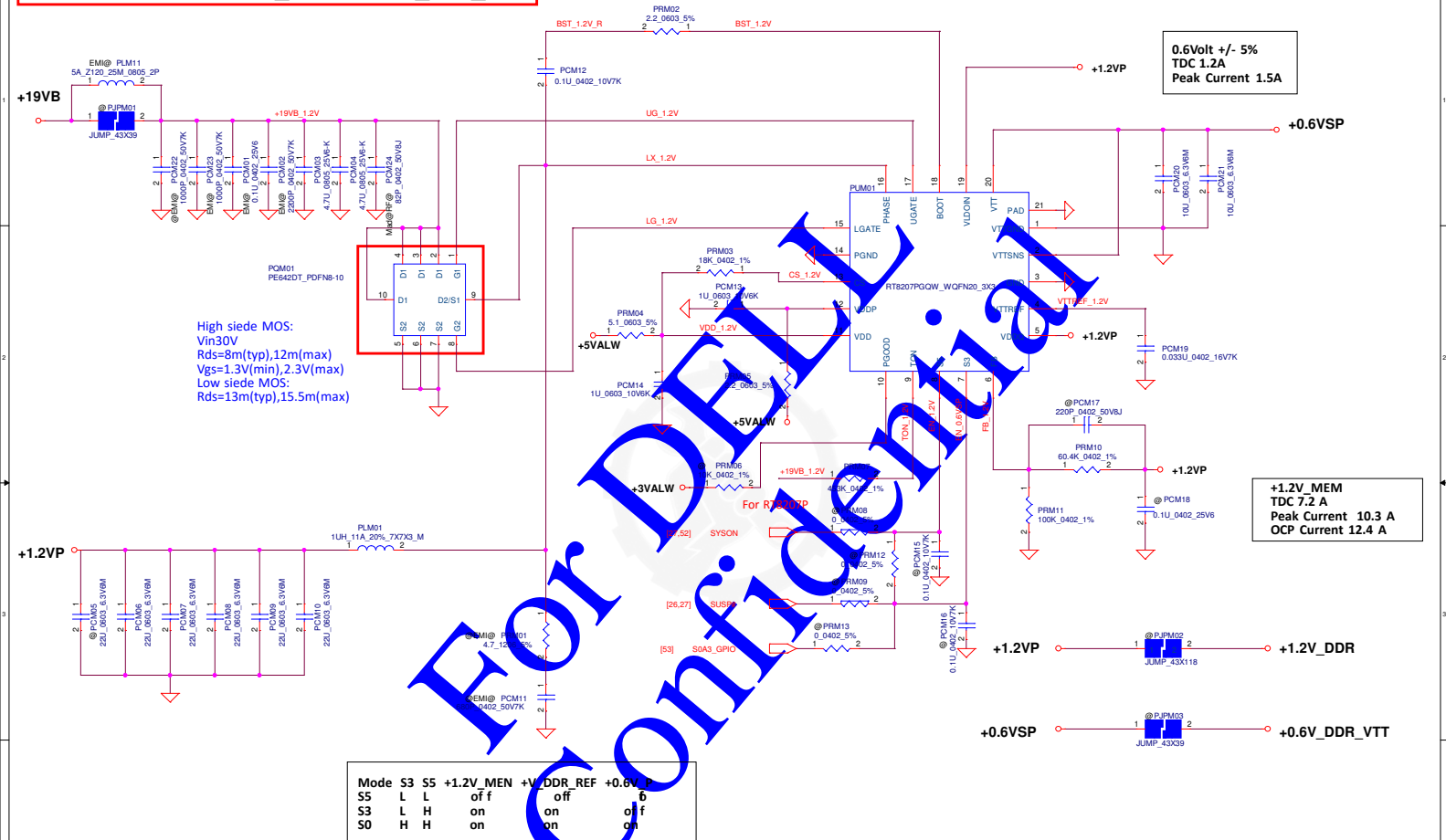
DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
PWR CHARGER			
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Main Func = 3.3VALWP/5VALWP



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				Rev 0 (000)
				Date: Thursday, November 09, 2017 Sheet 49 of 59

Main Func = +1.2V_DDR/+0.6V_DDR_VTT



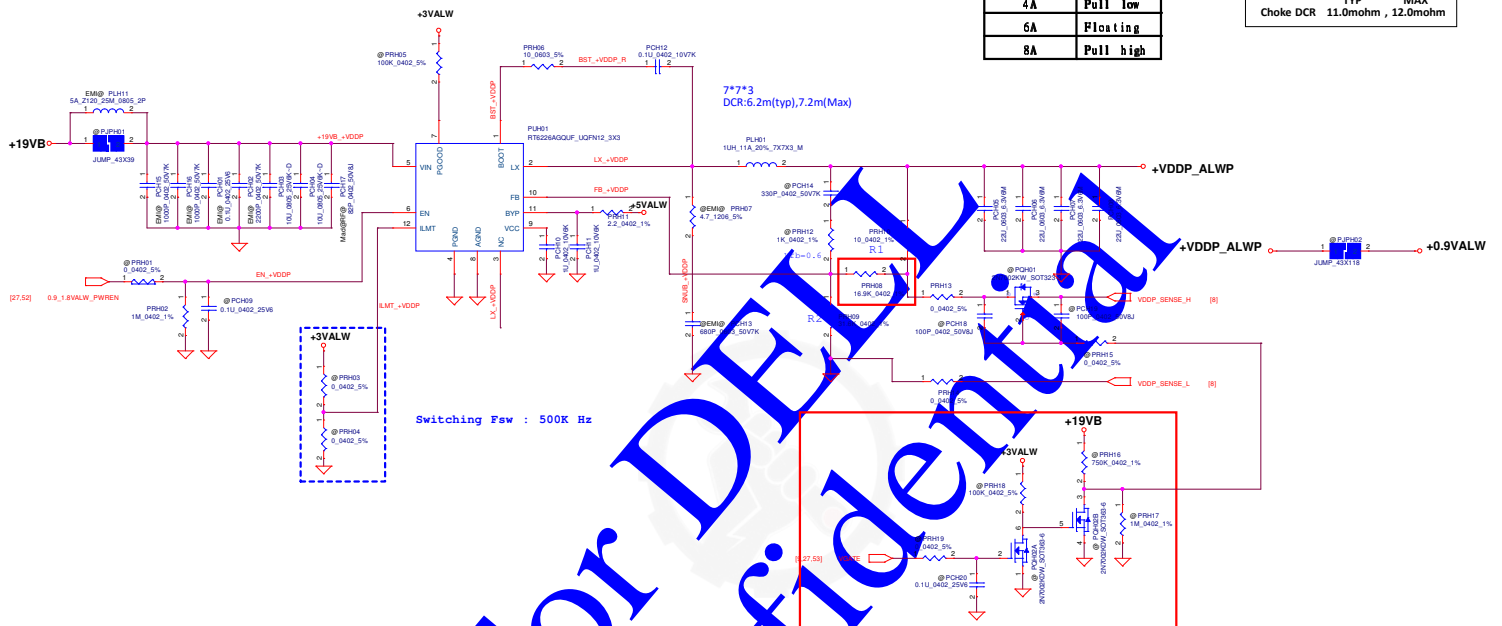
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Date: Thursday, November 06, 2017				Sheet 50 of 59

Main Func = +VDDP_ALWP

The current limit is set to 4A, 6A or 8A when this pin is pull low, floating or pull high

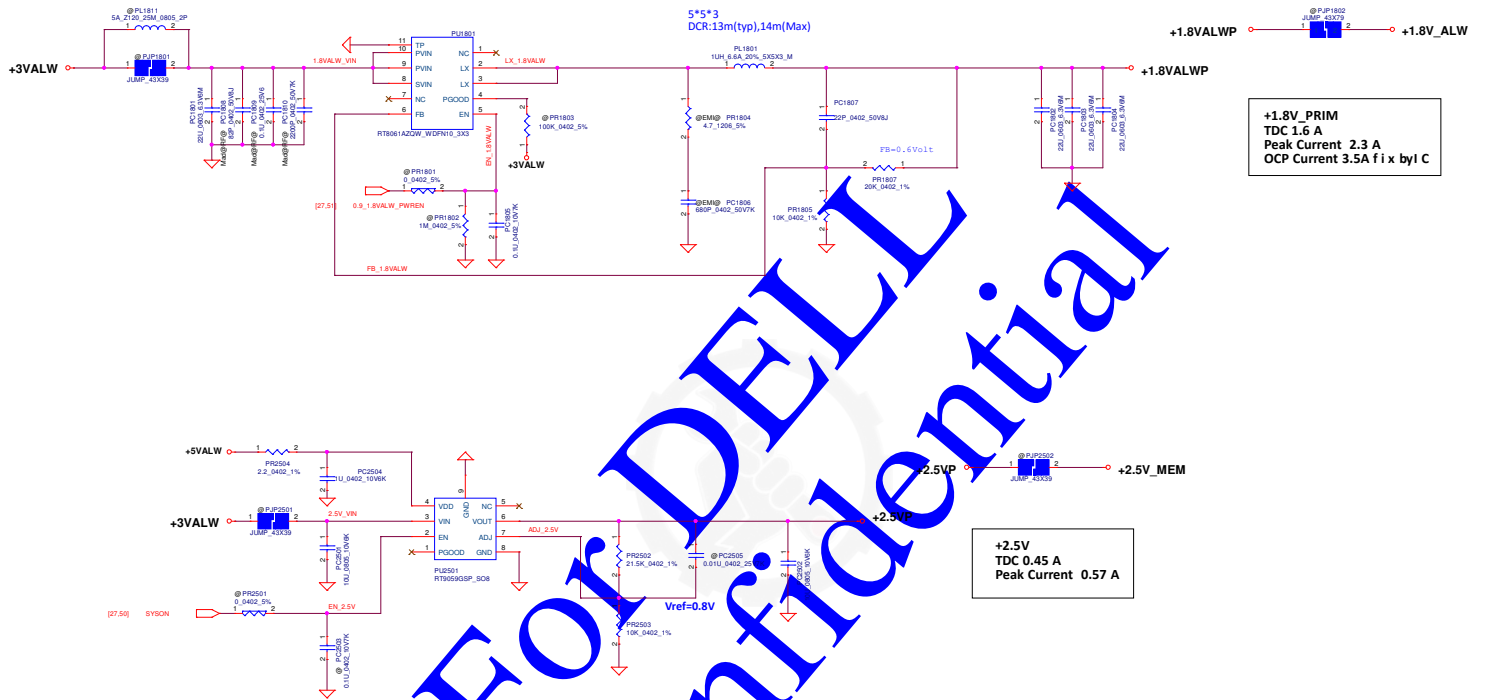
OCF setting	ILMT(pin3)
4A	Pull low
6A	Floating
8A	Pull high

+VDDP_ALWP
TDC 4 A
Peak Current 5 A
OCF Current 6 A Fix by IC
TYP MAX
Choke DCR 11.0mohm, 12.0mohm



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Issued Date	2015/03/23	Deciphered Date
2014/12/15		Rev
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Docu	Number	300
Ver	1	1
Ver	1	1

Main Func = +1.8VALWP / +2.5VP



+1.8V PRIM
TDC 1.6 A
Peak Current 2.3 A
OCP Current 3.5A fix by I C

+2.5V
TDC 0.45 A
Peak Current 0.57 A

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Rev	C	Document Number		REV
300				300
Notes	Noradex, November 05, 2017		Sheet	13 of 13

```
APU_VDDSOC
TDC 10A
Peak Current      13A
OCP current       19A

FSW=400kHz
```

LD800 (DCR:0.67m \pm 5 %)

```

APU_VDDCORE (FP5)
TDC 35A
Peak Current 45A
OCP current 57A

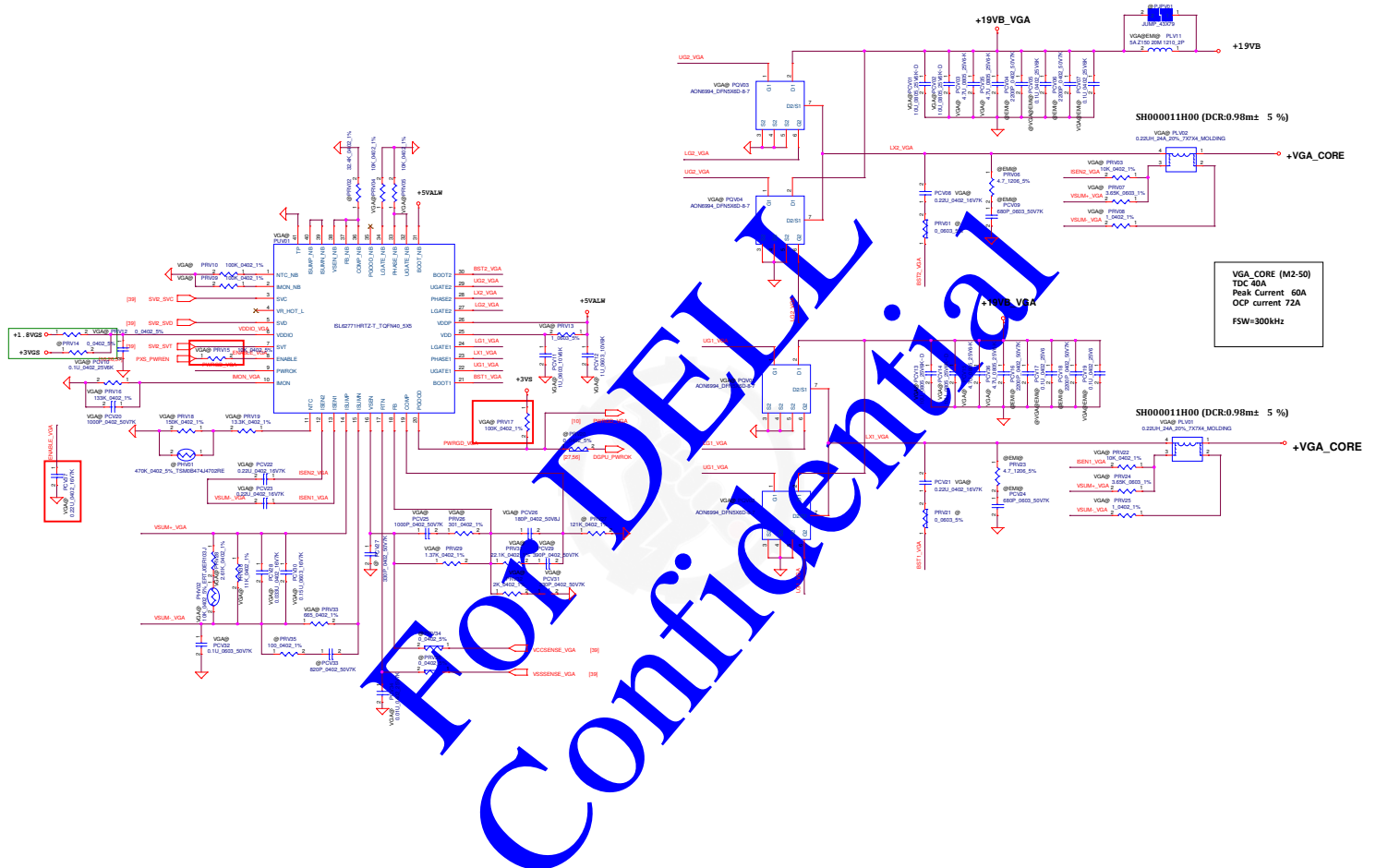
FSW=400kHz

```

LD800 (DCR:0.67m \pm 5 %)

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2015/004		2015/004		PWR APU CORE/APU CORE NB	
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				Date: Thursday, November 03, 2017 Sheet: 03 of 03	

Main Func = VGA CORE

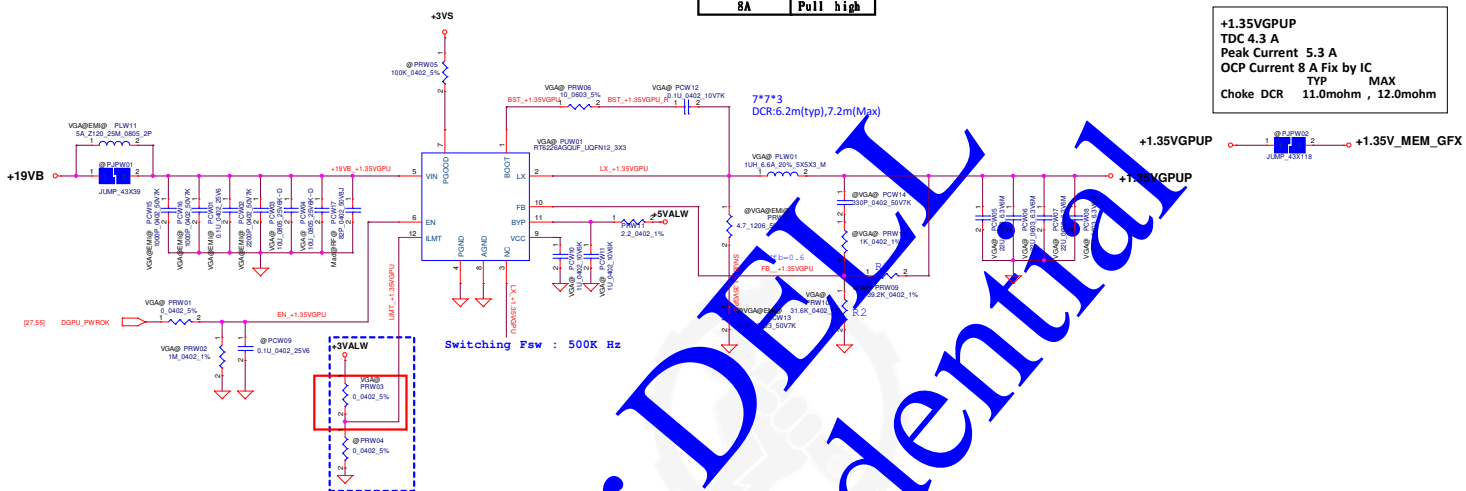


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				Doc. Name	Power Management	Rev. 1.0

Main Func = +1.35VG PUP

OCP setting	ILMT(pin3)
4A	Pull low
6A	Floating
8A	Pull high

+1.35VGPUP
TDC 4.3 A
Peak Current 5.3 A
OCP Current 8 A Fix by IC
Choke DCR TYP MAX
 11.0mohm , 12.0mohm

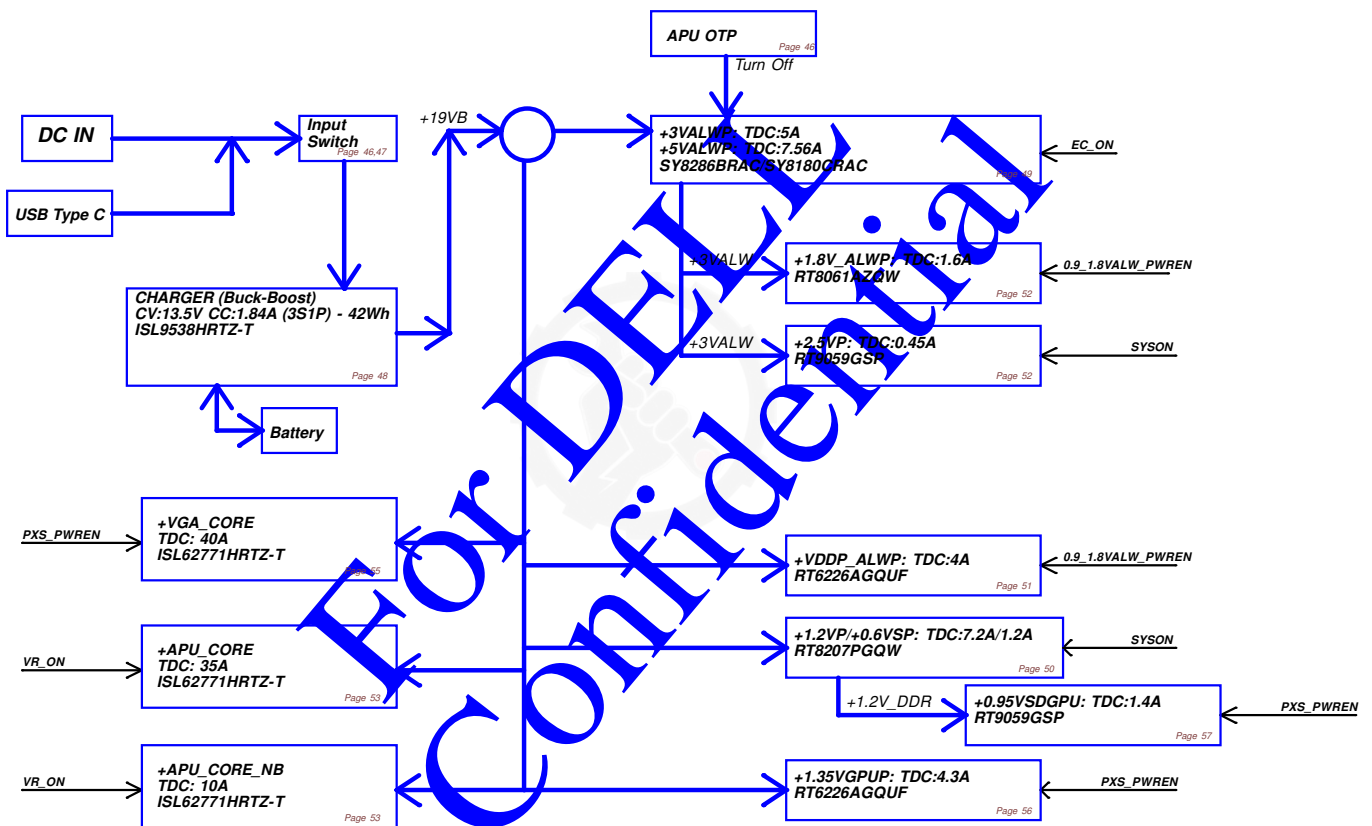


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Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2015/03/23	Deciphered Date	2014/12/15	PWR +0.95VSDGPU	
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Size	A		Quantity	1	Rev
Created	2007/05/07		Isocal	47	58

Power block



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title	
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				Date	Thursday, November 09, 2017
				Sheet	58 of 58

Version Change List (P. I. R. List)

<i>Item</i>	<i>Page #</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>	<i>Rev.</i>
1	P46	PWR	20170704	COMPAL	EMI test result for change capacity	change PC2,PC4 from 0.1u to 2200p	0.2 (X01)
2	P55	PWR	20170704	COMPAL	Request by EE for adjust DGPU sequence	change PRV15 from 0 to 10K and add PCV37 0.22u	0.2 (X01)
3	P48	PWR	20170704	COMPAL	support FTRD 1.6 and LPS from EC request	change PRV15 from 0 to 10K and add PCV37 0.22u	0.2 (X01)
4	P47	PWR	20170704	COMPAL	add fast close MOS	pop PQS06,PQS07,PQS13,PRS10,PRS15,PRS18,PRS36,PRS37,PRS38,PRS40.PRS41	0.2 (X01)
5	P46	PWR	20170710	COMPAL	for LPS SW solution	add PQ20	0.2 (X01)
6	P51	PWR	20170717	COMPAL	adjust output to 0.9V by EE request	change PRH08 from 10.7K to 15.8K	0.2 (X01)
7	P46	PWR	20170917	COMPAL	follow Intel design	pop PR53 and unpop PR51	0.3 (X02)
8	P46	PWR	20170917	COMPAL	follow Intel design	unpop PC20,PQS11,PRS30,PQS20 add PR100 1M	0.3 (X02)
9	P54	PWR	20170918	COMPAL	for PSI_Dynamic test with AMD validation	pop PCA106,PCA107	0.3 (X02)
10	P48	PWR	20170918	COMPAL	follow Intel design	unpop PCB46	0.3 (X02)
11	P51	PWR	20170918	COMPAL	for VDDP_Static test with AMD Validation	change PRH08 from 15.8K to 16.9K	0.3 (X02)
12	P46	PWR	20170920	COMPAL	follow Intel design	change PC7,PG10 from 0.1U_10V to 0.1U_50V	0.3 (X02)
13							

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Issued Date	2015/12/22	Deciphered Date	2017/01/31	Title
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				X00
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DVT1 change list

BOM change list

BOM Change								
Item		Date	Page	Part reference	Original CPN	New CPN	Change description	Reason
1		2017/6/2	33	RT52,RT53			bom structure from typec@ change to @	fix the typec i2c signal about DP out
2		2017/6/3	27	RE6			bom structure from nottypec@ change to pop always	fix dead battery auto wakeup
3		2017/6/3	27	RE508			bom structure from typec@ change to @	fix dead battery auto wakeup
4		2017/6/19	27	RE9	SD034000080	SD034150280	0 ohm change to 15K	EC board id(UMA)
5		2017/6/19	27	RE9	SD034120280	SD034200280	12k change to 20K	EC board id(DSC)
6		2017/6/20	9	RC29,CC7,RC700			change to pop(PCIE_RESET_0)	fixed pcie rst signal
7		2017/6/20	9	RC704,CC100,RC701			change to unpop(PCIE_RESET_1)	pcie rst_1 signal code not ready
8		2017/7/6	10	C796	SE07156AD80	SE07147AC80	change part from 5.6P to 4.7P	fixed crystal accuracy
9		2017/7/6	10	C797	SE07156AD80	SE000011R00	change part from 5.6P to 3.9P	fixed crystal accuracy
10		2017/7/6	9	D5,D6		SCS000002Z00	add part (diode)	fix Panel will flash white screen when press power button (Bits333224)
11		2017/7/12	29	Q26		SB000000DH00	add part (dual mos) reserve	follow loki intel led design
12		2017/7/12	29	R82,R83		SD028100380	add part(100K) reserve	follow loki intel led design
13		2017/7/12	29,34	R800,R562		SD028000080	add part(0 ohm)	follow loki intel led design
14		2017/7/12	23	CU38,CU39,CU40,CU41		SE00000P700	add part 0.33U	follow AMD require to add 0.33U Cap
15		2017/7/12	23	CU7,CU8,CU15,CU16	SE102104K00	SE095224K00	change part(0.1U to 0.22U)	follow AMD require to change to 0.22U Cap
16		2017/7/13	10	RC449	SD028330A80	SD028220A80	change part 33 ohm to 22 ohm	follow AMD SCL 1.04

GPIO change list

Signal for PCH				
Date	GPIO	Pin Definition		Reason
		R0.1(X00)	R0.2(X01)	
2017/6/3	AGPIO11	NC	MEM_ERROR_A	Memory error detection(Bits334733)
2017/7/4	AGPIO12	NC	MEM_ERROR_B	Memory error detection(Bits334733)
2017/7/4	EGPIO 70	NC	VBIOS_ID1	old GPIO SW no support
2017/7/10	AGPIO89	PXS_RST#	NC	fixed GPU Yellow bang
2017/7/10	AGPIO90	PXS_PWREN	KB_DET#	fixed GPU Yellow bang
2017/7/10	AGPIO86	PWRGD_VGA	NC	fixed GPU Yellow bang
2017/7/10	EGPIO 140	KB_DET#	PXS_RST#	fixed GPU Yellow bang
2017/7/10	EGPIO 141	NC	PXS_PWREN	fixed GPU Yellow bang
2017/7/10	EGPIO 143	NC	PWRGD_VGA	fixed GPU Yellow bang
KBC ENE 9022				
Date	GPIO	Pin Definition		Reason
		R0.1(X00)	R0.2(X01)	
2017/6/3	AGPIO0	NC	MEM_ERROR_A	Memory error detection(Bits334733)
2017/7/4	AGPIO39	NC	MEM_ERROR_B	Memory error detection(Bits334733)

Design change list

Design Change					
Item	Date	Page	Part reference	change description	Reason
Based on EVT					
1	2017/6/2	29		BATT_CHG_LED from R68.2 to R69.2 ,BATT_LOW_LED from R69.2 to R68.2	correct led color indication
2	2017/6/19	32		DT3-DT10 change footprint	meet DFB
3	2017/6/29	33		JUSBC1 change footprint	meet DFB
	2017/7/6	9		add D5,D6	fix Panel will flash white screen when press power button (Bits333224)
4	2017/7/11	36		JCRT from 20P coaxial to 16P ZIF	follow loki intel
5	2017/7/12	23		add RX cap footprint for usb compatible	follow AMD require
6	2017/7/12	29,34		add nvme led status circuit(reserve)	follow loki intel

DVT2 change list

BOM change list

BOM Change								
Item		Date	Page	Part reference	Original CPN	New CPN	Change description	Reason
1		2017/9/4	32	D2	SCA00001G00		unpop	follow ESD require
4		2017/9/4	27	RE9	SD034150280	SD034270280	15K change to 27K	EC board ID
5		2017/9/4	27	RE9	SD034200280	SD034330280	20K change to 33K	EC board ID
12		2017/9/4	11	RC801	SD028100580		add 10M	follow factory require for RTC detect
13		2017/9/4	11	QC27	SB00000EN00		add mos	follow factory require for RTC detect
14		2017/9/4	9	RC6130	SD028100280		add 10K	follow factory require for RTC detect
15		2017/9/8	18	CA50,CA51	SE071100J80		change to pop	follow EMI require
16		2017/9/18	33	RT132,RT133	SD028000080		add 0 ohm	follow SCL1.05

GPIO change list

Signal for PCH									
Date	GPIO	Pin Definition		Reason					
		R0.2(X01)	R0.3(X02)						
	AGPIO7	NC	RTC_DET#	factory require					
	AGPIO76	SPI_IRQ#	NC	PSP related GPIO					
	AGPIO30	NC	SPI_IRQ#	PSP related GPIO					
	EGPIO121	BT_ON#	NC	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.					
	EGPIO120	NC	BT_ON#	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.					

Design change list

Design Change							
Item	Date	Page	Part reference	change description	Reason		
Based on DVT1							
1	2017/9/4	11	QC27,RC801,RC6130	add RTC coin battery detect circuit	for factory require		
2	2017/9/4	27	RE9	UMA form 15K to 27K, DIS from 20K to 33K	EC board ID		
3	2017/9/4	10,20	RC902	reserve (0 ohm)	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.		
4	2017/9/12			I2C0 change to I2C3	BITS332966 ULV-Loki-AMD: Lost some items in Touchpad setting.		
5	2017/9/18	33	RT132,RT133	add series resistor for APU_DP3_AUXP/APU_DP3_AUXN	follow SCL 1.05		